ACTIVITY REPORT
2022-2023

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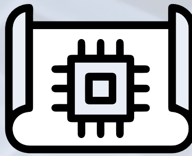
The access point to develop electronic components and systems

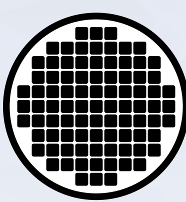
2022 at a glance

731 submitted designs



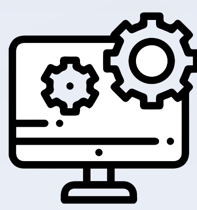
25 training courses

40 webinars on youtube



18 foundries in the technology portfolio

17 design tool vendors



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FOREWORD

Dear customers, colleagues and friends,

As always, we look forward to sharing with you the results we achieved last year. This time, we are doing it with mixed feelings. After the steady yearly growth of the number of fabricated designs, we see it has declined for the first time in a decade. We attribute it to multiple reasons. First of all, the EUROPRACTICE consortium partner in France CMP had to stop fabrication activities at STMicroelectronics, ams and CEA-Leti due to administrative reasons. Since ST is the most popular European foundry in our portfolio, it has significantly affected our results. We are glad to inform you that this issue has been resolved as a new French MPW service, CIME-P, was created in October 2022 and joined the consortium reopening the access to fabrication services in these foundries. Among other factors responsible for the decline, we must mention the geopolitical circumstances, which led to the end of our relations with Russia and considerably restricted our operations with China.

So what is this decreased **number of submitted designs in 2022**? It is still a good result: **731**, where most of the designs (73%) were prototyped by European academia and industry. Like previous years, the largest share of designs was fabricated in TSMC, the leading foundry for the global industry. It is followed by GlobalFoundries, which increased its numbers by nearly a third, and by a European R&D fab IHP, whose numbers have also shown good growth. We are pleased to see that advanced technologies are becoming increasingly popular among our users: the number of designs in the 22nm FDSOI technology of GlobalFoundries has increased from 50 in 2021 to 88 last year. In addition, the share of prototypes in FinFET technologies of TSMC and GlobalFoundries remains at a good level and slowly rises.

The **biggest highlight** of last year was no doubt the lifting of COVID-19 limitations and the return of face-to-face events and training courses. Together with physical events, we kept organising online training that is often easier to attend. Over the last year, we delivered in total 25 training courses that were attended by more than 300 delegates. We have also continued EUROPRACTICE webinars, where a new series was dedicated to the 2D Experimental Pilot Line (2D-EPL), whose Graphene processes developed at AMO and VTT are now accessible through EUROPRACTICE. All our webinars are available on the YouTube channel of EUROPRACTICE services, which already has nearly 50000 views.

Another great news is that **Key Digital Technologies Joint Undertaking (KDT JU) have supported EUROPRACTICE** through a funded project RETICLES: Research, Entrepreneurship, Training, IP-exchange & Chip pLatform of EUROPRACTICE Services. This will allow us to continue the EUROPRACTICE platform until September 2025 and extend it with new services and technologies to nurture the further growth of the design ecosystem in Europe and provide a breeding ground for deep-tech start-ups.

In 2023, EUROPRACTICE will continue providing you with high-quality services. We hope that the newly started year will allow us to fully resume our operations, reopening access to all the foundries in our portfolio. And of course, we are looking forward to seeing you at the finally restarted physical events.

We thank all of you – our academic and industrial customers, our technology and design tool suppliers – for supporting our services, and we wish you all a productive and successful 2023.

Looking forward to supporting your innovative projects and creating more success stories together,
Your EUROPRACTICE team at imec, UKRI-STFC, Fraunhofer IIS, CIME-P and Tyndall

TABLE OF CONTENTS

Foreword 1

EUROPRACTICE Services: The access point for electronic components and systems 3

- EUROPRACTICE business model 4
- Affordable access to state-of-the-art CAD tools 5
- Easy access to prototyping 6
- Multi-Project-Wafer and mini@sic runs 6
- Technology portfolio 2023 7
- Multi-Level Mask single user runs 8
- Packaging 8
- Advanced packaging and smart system integration 9
- From prototypes to volume production 10
- Training in design tools and technologies 11
- Webinars 12
- Outreach and communication 13

Results 2022: MPW prototyping services 15

User Stories on Prototyped Designs 18

EUROPRACTICE Membership / List per Country 60

EUROPRACTICE SERVICES

THE ACCESS POINT FOR ELECTRONIC COMPONENTS AND SYSTEMS

EUROPRACTICE offers a platform with a full range of services to design, fabricate, package and integrate microelectronic circuits. For nearly 30 years, we have supported our customers in all critical steps on the way from prototype design to volume production.

OUR OFFER

- Affordable access to industry-standard design tools, especially for European academia and start-ups
- Prototyping in multiple technologies, such as ASICs, Photonics, MEMS and Microfluidics, via Multi-Project-Wafer (MPW) runs
- Smart system integration and advanced packaging
- Route to volume production, including test and characterization services
- Training courses and webinars in design flows and various technologies

OUR STORY

EUROPRACTICE was launched by the European Commission in 1995 succeeding its forerunner EUROCHIP (1989-1995). The service aimed to enhance European industrial competitiveness in the global marketplace by opening easy access to design tools and IC prototyping.

Since its creation, EUROPRACTICE has bridged the gap between academia and industry in the high-tech world by supporting more than 600 European universities and research institutes, and over 300 SMEs.

In the coming three years, Key Digital Technologies Joint Undertaking (KDT JU) will support EUROPRACTICE through a funded project **RETICLES**: Research, Entrepreneurship, Training, IP-exchange & Chip pLatform of EUROPRACTICE Services.

The project will nurture the further growth of the design ecosystem in Europe, building on the existing EUROPRACTICE platform and extending it with new services and technologies.

In RETICLES, design activities will be facilitated through design reuse and establishing IP exchange repositories. Design in the most advanced technologies will be enabled with the appropriate CAD tools and new cloud-based solutions. The creation of smarter integrated systems will be stimulated through advanced system integration of dissimilar semiconductor technologies and chiplets. A breeding ground for deep-tech start-ups will be provided by supporting the subsequent commercialisation of academic research and lowering the barrier to advanced design tools, leading-edge semiconductor technologies and bespoke training.

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EUROPRACTICE BUSINESS MODEL

The EUROPRACTICE business model is based on a coordinated brokerage service for industrial companies and academic institutions who look for affordable and easy access to technologies in the domain of electronic smart systems. The service builds on the many years' experience of five consortium partners: imec, UKRI-STFC, Fraunhofer IIS, CMP and Tyndall.

EUROPRACTICE offers customers technology access through a vast network of suppliers that includes design-tool and IP-library vendors, foundries, assembly and test houses – who all provide state-of-the-art industry-grade technologies.

Tools

IP

Fabrication

CAD

EUROPRACTICE

Academic Customers

Industrial Customers

Fig. 1: Schematic representation of the entire EUROPRACTICE ecosystem, depicting a central role of the EUROPRACTICE service as prime interface between the technology suppliers (on top) and the customers (at the bottom).

The overall concept is that EUROPRACTICE acts as the prime interface between the customers and the technology providers. Such a prime interface (or one-stop function) has advantages for both the supply and demand side of the value chain. It is schematically represented in Figure 1, where the supply side is depicted on top, the demand side at the bottom and EUROPRACTICE in the centre.

The supply side corresponds with the current service portfolio, where design tools are provided by design-tool vendors, IP by dedicated library vendors and fabrication services by various foundries. In addition, the portfolio is extended with emerging technologies typically offered by leading research institutes, and technologies brokered by other service providers (such as CMC in Canada for Silicon Photonics by AMF).

Although EUROPRACTICE represents a large customer base, it is considered as one user by its suppliers. Design tool vendors, IP-vendors and foundries need to deal only with EUROPRACTICE to have their products and technologies promoted and securely distributed all over Europe. Thanks to this, EUROPRACTICE has been able to negotiate technology access on very favourable terms for its customers. This would not be possible when operating on a national level with only few users. Since the service functions on a pan-European level, the know-how and experience have only to be built up once.

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AFFORDABLE ACCESS TO STATE-OF-THE-ART CAD TOOLS

EUROPRACTICE has negotiated lower prices with the major design tool vendors world-wide, as well as with IP and programmable device vendors. Consequently, European academic institutions can access EUROPRACTICE licenses of the most advanced EDA/CAD tools for a wide range of electronic system (including IC, MEMS, Photonics etc.) design at affordable prices for education and non-commercial research. The design tools are made available in vendor specific functional bundles that are cost effective, easy to install and are enhanced annually under maintenance contracts to add new functionality. In addition, the EUROPRACTICE service provides an infrastructure to allow its Members to access EDA/CAD vendor material, such as training material, on a scale which otherwise would not be possible.

The current EUROPRACTICE network of European academic institutions is the largest network in the world having a unique and uniform tool base for electronic system, IC, MEMS and Photonics design. Access to these advanced CAD tools allows our customers to participate in EC-funded projects, ranging from IP block and component design to the design of complete systems.

DESIGN TOOLS FOR SMEs

European SMEs can access certain design tools at low cost via EUROPRACTICE in order to produce a proof-of-concept IC to demonstrate their IP/product. The resultant IP can then be fully commercialized for an additional agreed fee. The SME gains access to an industry-standard full IC design flow, suitable for all IC technologies.

EUROPRACTICE works flexibly with academic institutes and SMEs to facilitate effective innovation. For instance, we have mechanisms in place if an academic institute has developed a design using EUROPRACTICE tools and subsequently wishes to exploit this design commercially, either via a spin-out or by transferring the IP to an existing SME.

EASY ACCESS TO PROTOTYPING

It is challenging for small companies, academic and research institutions to obtain access to foundry fabrication lines since they often need a high level of technical support and require only a small-volume production for prototyping purposes. If they choose to work directly with a commercial foundry, the manufacturing costs will be very high.

This is when EUROPRACTICE comes into play. We help significantly reduce fabrication costs by opening access to Multi-Project-Wafer (MPW) runs and Multi-Level-Mask (MLM) services for prototyping and volume production respectively.

In addition, EUROPRACTICE offers a wide choice of technologies of world-leading foundries together with technical support and training.

TECHNOLOGY PORTFOLIO

At the beginning of 2023, the EUROPRACTICE portfolio includes a broad range of technologies, such as ASIC processes ranging from 2µm to 7nm, MEMS, Silicon and Glass Photonics, and Microfluidics. The ASIC processes have various options, including digital logic, RF, mixed-signal and high-voltage. Traditionally, EUROPRACTICE focuses on technologies from European-based companies as 14 of the 18 foundries have manufacturing facilities in Europe.

Over the past year, EUROPRACTICE promoted Graphene technologies of AMO and VTT developed in the 2D Experimental Pilot Line (2D-EPL).

At the beginning of 2023, the barrier to TSMC 16nm and 7nm FinFET technologies has been lowered for EUROPRACTICE-member universities thanks to the TSMC FinFET University Program.

TSMC University FinFET Program
EUROPRACTICE-member universities can now access the TSMC N16 FinFET technology at special pricing. Selected universities can also gain access to the cutting-edge TSMC N7 FinFET.

MULTI PROJECT WAFER AND MINI@SIC RUNS

By combining several designs from different customers onto the same mask set of a prototype run, known as Multi-Project-Wafer (MPW) run, the high cost of the mask set and the fabrication process is shared among the participating customers.

Fabrication of prototypes can therefore be as low as 5% to 10% of the cost of a wafer run for only one dedicated customer. A limited number of IC prototypes, typically 20-50, are delivered to the customer for evaluation, either as naked dies or as encapsulated devices. Only prototypes from fully qualified wafers are taken to ensure that the chips delivered will function "right first time". To achieve this, extensive Design Rule and Electrical Rule Checkings are performed on all designs submitted to the Service.

Since most of the designs fabricated for educational purposes are much smaller than the minimum block size on regular MPW runs, the concept of **mini@sic** was introduced in 2003. This solution allows to further lower prototype fabrication costs compared to standard MPW runs. The mini@sic principle is based on the following methodology: Several times per year, a foundry standard MPW block is bought and resold in smaller and cheaper sub-blocks or mini@sics. This program has been extended over the years and currently includes selected technologies from GlobalFoundries, IHP, TSMC, UMC and X-FAB.

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TECHNOLOGY PORTFOLIO 2023

Graphene process of AMO and VTT

ams OSRAM

ams 0.35µm CMOS C35B4C3
ams 0.35µm CMOS C35OPTO + BARC Diode option
ams 0.35µm HV CMOS H35B4D3
ams 0.35µm SiGe-BiCMOS S35
WLSCP for ams C35B4C3
ams 0.18µm CMOS atC18c

EM Microelectronic 0.18µm EMALPC18 logic

GF SiGe 8XP
GF 130nm BCDlite-Gen2
GF 55nm BCDlite 55nm BCDlite
GF 45nm SPCLO Si-Photonics
GF 45RFSOI
GF 28nm SLPe
GF 22nm FDSOI
GF 12nm LP+

IHP SGB25V 0.25µm SiGe:C
IHP SG25H3 0.25µm SiGe:C
IHP SG25H5_EPIC (BiCMOS + Photonics)
IHP SG25 PIC (Photonics)
IHP SG13S 0.13µm SiGe:C
IHP SG13C 0.13µm SiGe:C
IHP SG13G2 0.13µm SiGe:C
IHP SG13G2Cu FEOL + Cu BEOL option
IHP SG13SCu FEOL + Cu BEOL option
IHP BEOL SG13
IHP SG13S + MEMRES Module
IHP SG13G3Cu 0.13µm SiGe:C

ST 28nm CMOS28FDSOI
ST 55nm BiCMOS055
ST 65nm CMOS065
ST 130nm BiCMOS9MW
ST 130nm HCMOS9GP
ST 130nm HCMOS9A
ST 0.16µm BCD8sP
ST 0.16µm BCD8s-SOI

TSMC 0.13µm BCD+ (12")
TSMC 0.13µm CMOS Log/MS/RF (G, LP)
TSMC 90nm CMOS Log/MS/RF (G ,LP)
TSMC 65nm CMOS Log/MS/RF (G, LP)
TSMC 40nm CMOS Log/MS/RF (G, LP)
TSMC 28nm CMOS Log/RF HPC/HPC+
TSMC 16nm CMOS Log/RF FinFET Compact
TSMC 7nm CMOS Log/RF FinFET

UMC L180 Logic GII, MM/RF
UMC L110AE Log/MM/RF
UMC L55N Log/MM/RF (SP)
UMC L65N Log/MM/RF (LL)
UMC 40N Log/MM – LP
UMC 28N Log/MM – HPC

X-FAB XH035 0.35µm HV
X-FAB XH035 Noble Metal
X-FAB XH018 0.18µm HV NVM E-Flash
X-FAB XT018 0.18µm HV SOI
X-FAB XS018 0.18µm OPTO
X-FAB XP018 0.18 µm NVM
X-FAB XR013 0.13µm RF SOI
X-FAB XMB10 MEMS

AMF Si-Photonics

CEA-leti Si-Photonics Si-310
CEA-Leti SiN-Photonics Si_3N_4-800
CEA-Leti MAD200 130nm NVM

CORNERSTONE Si-Photonics 220 passives/actives
CORNERSTONE Si-Photonics 340 passives
CORNERSTONE Si-Photonics 500 passives
CORNERSTONE SiN-Photonics
CORNERSTONE Suspended-Si

Fan-Out Wafer-Level Packaging
4H-SiC CMOS High Temperature Technology

imec

imec GaN-IC on SOI 200V/ 650V
imec Si-Photonics Passives+
imec Si-Photonics ISiPP50G

Glass microfluidics

LNX SiN-Photonics TriPleX VIS
LNX SiN-Photonics TriPleX 550
LNX SiN-Photonics TriPleX 850

MEMSCAP PolyMUMPS
MEMSCAP SOIMUMPS
MEMSCAP PiezoMUMPS

Glass-Photonics IC ioNext-NIR
Glass-Photonics IC ioNext-VIS
Glass-Photonics IC WAFT

PiezoMEMS Single electrode layer stack
PiezoMEMS Dual electrode layer stack

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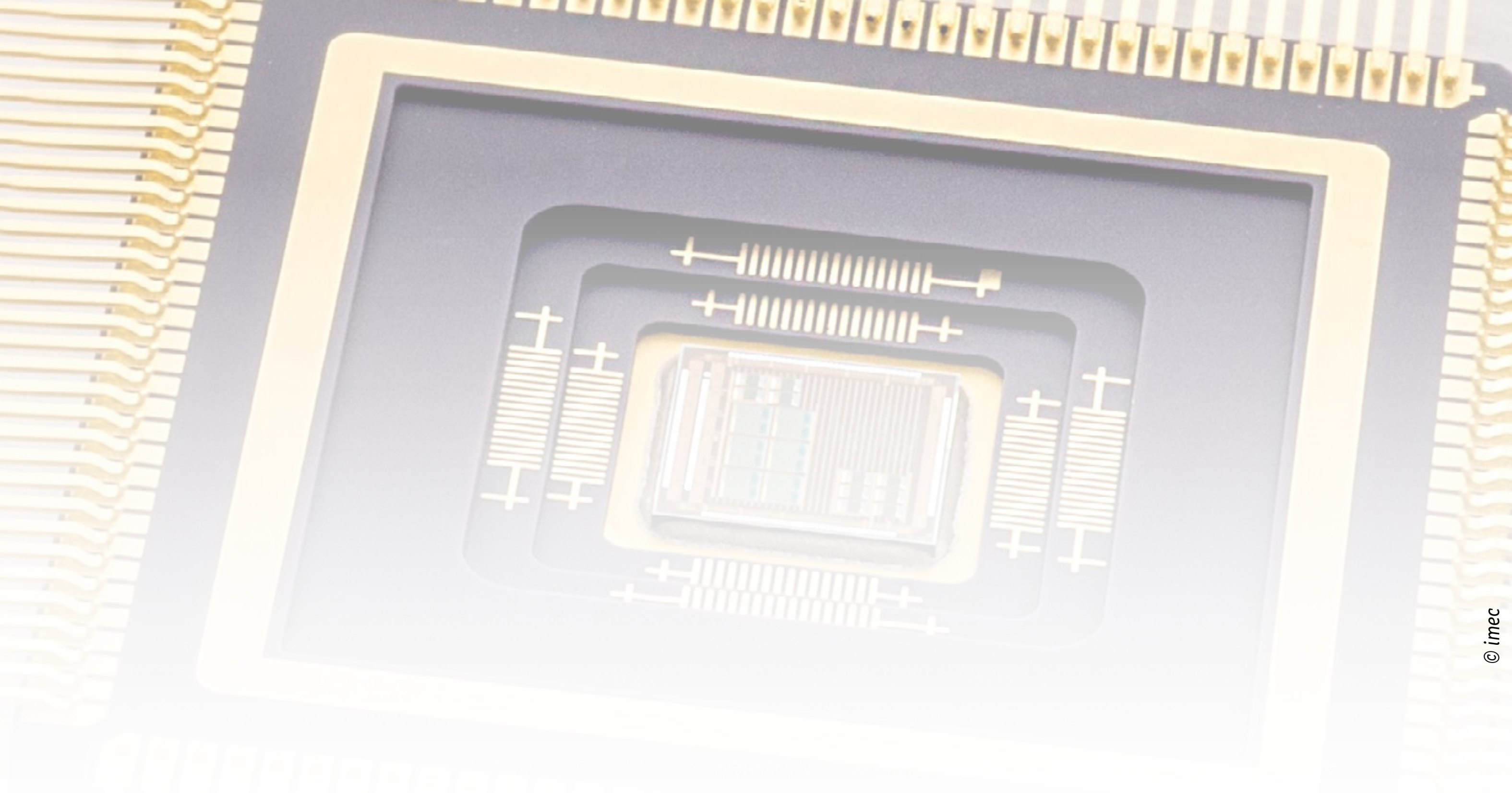


MULTI-LEVEL MASK SINGLE USER RUNS

Another technique to reduce the high mask costs is called Multi-Level Mask (MLM). With this technique the available mask area (for example 20mm × 20mm field for stepper equipment) is typically divided in four quadrants (4L/R : four layers per reticle) whereby each quadrant is filled with one design layer. As an example: one mask can contain four layers such as nwell, poly, ndiff and active. The total number of masks is therefore reduced by a factor of four. By adapting the lithographical procedure, it is possible to use one mask four times for the different layers by using the appropriate quadrants. This technique allows to significantly decrease the mask costs.

The advantages of using MLM single user runs are:

- lower mask costs
- an MLM run is organized for one customer
- it can be scheduled for any date since it does not depend on regular MPW runs
- a customer receives a few wafers, resulting in a few hundreds of prototypes

The MLM technique is preferred over MPW runs when the chip area becomes large and when the customer would like to get a higher number of prototypes. When the prototypes are successful, this mask set can be used under certain conditions for low-volume production.

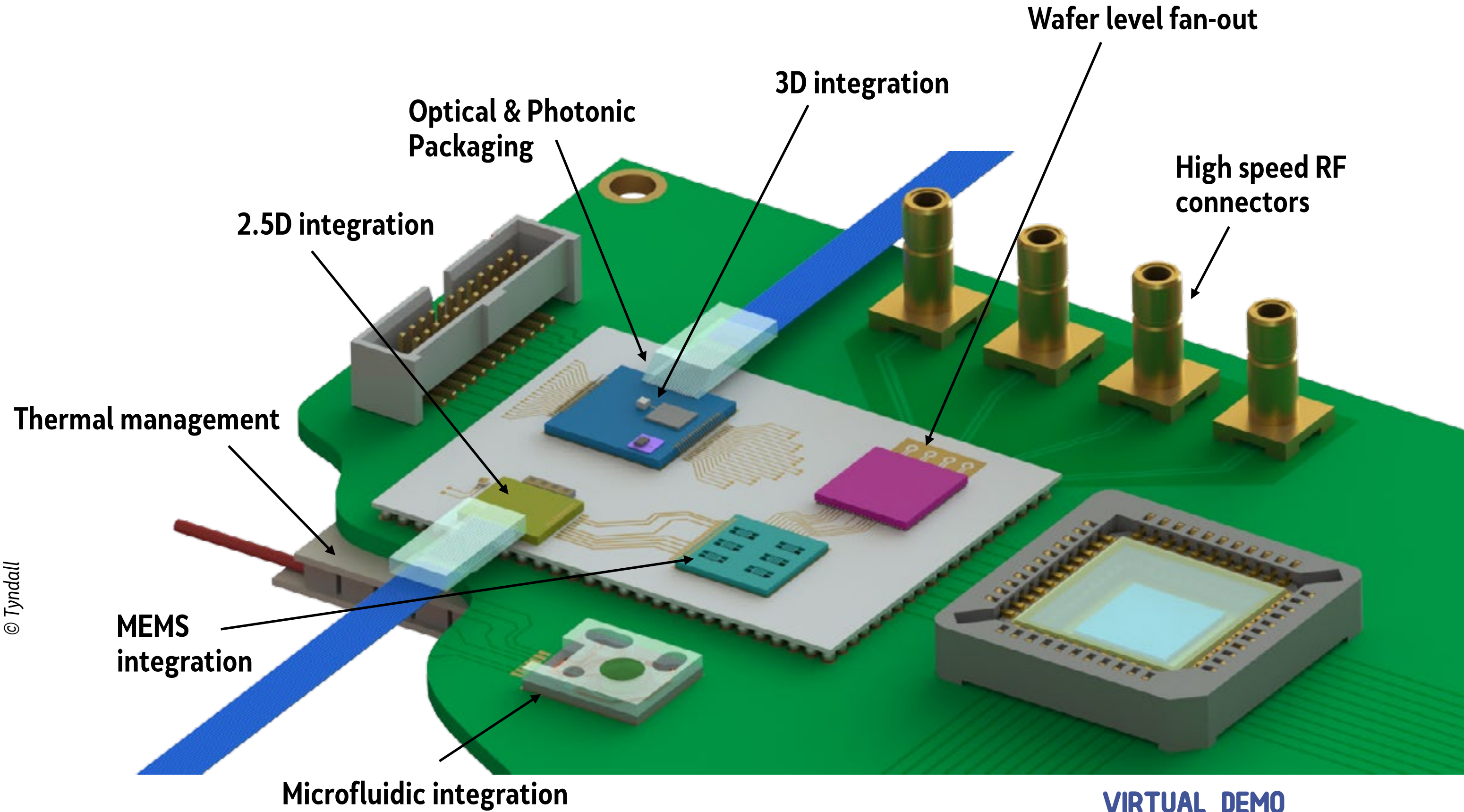
MLM runs are available for technologies from IHP, X-FAB and onsemi. As of 2022, onsemi does not offer MPW runs anymore and focuses on MLM.

PACKAGING

As a standard, EUROPRACTICE delivers unpackaged, untested prototype chips. However, EUROPRACTICE offers a low-cost, flexible and coordinated packaging service using industrial qualified packaging houses. A wide variety of **ceramic and plastic packages** are available, ranging from DILs (Dual-in-line) to PGAs (Pin Grid Array) and QFNs (Quad-Flat No-leads).

Side by side with world class partners and our long-term agreements, EUROPRACTICE boosts the deployment of your chip backend operations activities. This business environment is strengthened by a skilled team of in-house engineers who provide a reliable integrated service, from technical aspects up to logistics and supply chain management.

In addition, **photonics packaging** is offered by Tyndall. The photonics ecosystem continues to gather momentum attracting new users (from both academia and industry) and increasing the technical scope of the photonics offering via EUROPRACTICE. Finally, advanced packaging and system integration now complements EUROPRACTICE portfolio.



VIRTUAL DEMO

ADVANCED PACKAGING AND SMART SYSTEM INTEGRATION

There is a growing demand for advanced packaging and system integration in the semiconductor industry. This trend has been fuelled by the need of a wide range of applications for better integration of more functionalities in a system-on-chip (SoC) and system-in-package (SiP). System integration is a scientific and engineering challenge of combining a variety of technology modules, such as microsystems, microelectronics, optics, photonics, MEMS, microfluidics and combinations thereof. Examples of system integration in the semiconductor industry are vast, such as high-speed high-density datacom, artificial intelligence (AI), Internet of Things (IoT), bio-medical devices, sensors and many more.

Currently, the EUROPRACTICE portfolio is being extended with advanced packaging and system integration services enabling customers to realise complex multi-technology devices that can be upscaled from early-stage prototypes to volume manufacturing. This is achieved by adding specific processes or technologies in combination with the development of design rules and thereby facilitating advanced package design for system-on-chip integration.

EUROPRACTICE is showcasing the new system integration offer by means of virtual demonstrators, which are depicted on this page. They demonstrate how different building blocks or process modules make integration between multiple technologies possible. This covers advanced packaging of ASICs, photonics, MEMS, microfluidics and combinations of these technologies, from their design to their fabrication and integration.

System integration is made possible through EUROPRACTICE's unique access to a variety of specialized process modules, including 2.5/3D integration of ASICs and PICs through die stacking techniques using pick-and-place, flip-chip, BGAs, Cu pillars as well as silicon interposers. Access to wafer-level fan-out packaging is also provided, where dies from different sources or different technologies with varying thickness and size can be handled and packaged with one integration technology. Finally, add-on processes for noble metal finishes and microfluidic building blocks will be added to the technology portfolio, which are prerequisites for many bio-medical sensor devices. Most importantly, all solutions use industry-standard processes making them scalable to high volume and more cost effective.

FROM PROTOTYPES TO VOLUME PRODUCTION

Once successful ASIC prototyping has been completed based on the MPW principle, we can also provide a clear route to volume production (from low to mid-high volumes). During this upscaling process, you work closely together with one of the EUROPRACTICE partners, depending on the technology of your choice.

MIGRATION TO A FULL MASK SET

Based on a successful and validated prototype, the ASIC can be fabricated on a dedicated full mask set. One of the EUROPRACTICE partners takes care of the production of the first engineering wafers and organises the assembly in ceramic or plastic packages. Using their own bench tests, the designer can check the functionality of the ASIC produced on the full mask set.

DEVELOPMENT OF A TEST SOLUTION

When the device behaves according to the ASIC specifications, a test solution on an ATE (Automatic Test Equipment) platform is required to deliver electrical screened devices using a stable production test program. The test can be performed both on wafer level and on packaged devices. The goal is to screen the ASIC for manufacturing problems using the ATPG (Automatic Test Pattern Generation) and functional patterns. One of the EUROPRACTICE partners supports you during the development of single-site test solution as well as with a multi-site test solution when high-volume testing is required.

DEBUG AND CHARACTERIZATION

Before going into production, a characterisation test program checks if all the ASIC specifications meet the customer's expectations. Threshold values are defined for each tested parameter. The software tests all the IP blocks and functionalities in the ASIC, and the results are validated against the bench test results. A characterisation at Low (LT), Room (RT) and High (HT) temperature is performed on a number of (corner) samples together with statistical analysis (Cp and Cpk) to understand the sensitivity of the design against corner process variations.

QUALIFICATION

When the silicon is proven to be robust against process variations, the product qualification can start. Our partners can support you through the full qualification process using different kinds of qualification flows, including Automotive, Consumer, Industrial, Medical, Space, Military, Jedec and ESCC standards.
In this stage of the project, qualification boards must be developed for reliability tests and environmental tests.

YIELD IMPROVEMENT

EUROPRACTICE partners can perform yield analysis to determine critical points during the production and suggest the correct solution to maximise the yield. During the characterisation and qualification of the device on corner lots, the customer receives support in defining the final parameter windows. During the ramp-up phase, data of hundreds of wafers are analysed to check for yield incidents related to assembly and wafer production. The well-proven tool Examinator™ from Galaxy Semiconductor is used, enabling our engineers to perform fast data and yield analysis studies.

SUPPLY CHAIN MANAGEMENT

The responsible EUROPRACTICE partner will manage the full supply chain for you. This highly responsive service takes care of the planning processes with the different actors in the value chain during both engineering and production phases. Integrated logistics ensures the accurate achievement of the final delivery dates.

- **Ceramic and plastic assembly partners:** Alter Technology, Amkor Technology, ASE, Greatek Electronics, Integra Technologies, JCET, Kyocera, MAF, MSEI, QP Technologies, SERMA Microelectronics, Teledyne e2v
- **Wafer bumping partners:** ASE, Pactech
- **Photonics packaging:** Alter Technology, Bay Photonics, PHIX, PIXAPP, Tyndall
- **Test partners:** Alter Technology, Aptasic, ASE, EAG Laboratories, Salland Engineering, Microtest, Presto Engineering, RoodMicrotec
- **Failure analysis:** Eurofins MASER, RoodMicrotec
- **Library partners:** Aragio, ARM, Cadence, eMemory, Faraday, Synopsys
- **Rad test facility:** LLN, RADEF
- **Tape & Reel:** Reel Service
- **Long-term storage:** TÜV NORD GROUP
- **Wafer backend activities:** DISCO HI-TEC EUROPE

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TRAINING IN DESIGN TOOLS AND TECHNOLOGIES

EUROPRACTICE provides training courses targeting academic staff and PhD students from European universities and research institutes. Unlike training courses which address single topics or individual design tools, the EUROPRACTICE training courses typically address a design flow which makes these training courses an efficient way to acquire new knowledge and ideally suited to new PhD students and junior engineers with a need to quickly become productive with a design flow.

Since the courses are based on the EUROPRACTICE design tools, PDKs and Technologies, participants will be able to directly apply the techniques learnt on the training course when they return back to their own organization and make full use of the EUROPRACTICE infrastructure in their innovation, research and training.

Courses include a strong element of practical sessions where participants have an opportunity to extensively practice the concepts described in lectures, and have access to experts who can answer questions about the concepts, design tools or technology processes discussed on the course.

Where a design flow is well supported by multiple vendors and/or processes, multiple course variants are offered that reflect the typical practice within European industry.

Over the last year, 25 courses provided training to more than 300 delegates with 150 of these delegates being PhD students many of which will go on to become future industry and academic leaders.

40 videos with our recorded webinars are available on the official YouTube channel of EUROPRACTICE Services.

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WEBINARS

To introduce the constantly growing service portfolio and share valuable technology insights, EUROPRACTICE regularly develops and hosts highly successful webinars. These online events usually include informative presentations given by experts from world-leading companies, foundries or academic institutions, followed by a short Question & Answer session. All webinars are free of charge and open for a broad audience with different background.

At the beginning of 2022, we hosted a very popular webinar series Introduction to imec's MPW services. Later that year, we organised the following events:

Graphene and the 2D-EPL

This three-webinar series was created in collaboration with the 2D Experimental Pilot Line (2D-EPL). It was meant to introduce the EUROPRACTICE community to graphene and related material. The focus was on the processes developed at AMO and VTT, whose MPW runs were open to EUROPRACTICE users. We are currently preparing new webinars to continue the series in 2023.

Integrated Quantum Photonics

This online workshop presented key concepts of integrated quantum photonics, introduced the fabrication process of an open-source and license-free foundry CORNERSTONE, and gave participants an opportunity to get acquainted with the software design flow through a Luceda Photonics design tools live demo.

Since the very first webinar at the end of 2019, all EUROPRACTICE webinars have remained highly popular: 39 live-stream sessions were attended by 3232 delegates, followed by around 46706 views of the recordings on YouTube. Most webinars are organised in series that provide insights into different technologies, such as Microfluidics, MEMS, Flexible Electronics, Silicon-Photonics, and advanced Photonics packaging.

We encourage you to watch the recordings of our webinars on YouTube and to stay tuned for the new series to come.

OUTREACH AND COMMUNICATION

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Probably for everyone involved in outreach and communication activities, the greatest news of last year was the end of COVID-19 restrictions and the return of face-to-face events. However, we must admit that the months of isolation had also an upside making us more actively develop online communication channels to remain in touch with our customers. First of all, we have to mention here websites and social media.

WEBSITES

The **General Portal** europractice.com gives a good overview of a very broad and diverse EUROPRACTICE offer.
If visitors need further information on one of the aspects of our portfolio, it will redirect them to:

WHAT IS EUROPRACTICE?

EUROPRACTICE provides a critical infrastructure for Europe and services that enhance Europe's competitiveness in the global market place. In the high-tech world of ASICs and Smart Systems, EUROPRACTICE lowers the barriers for academia to exploit the latest technologies in their research, innovation and the training of the large numbers of highly-skilled graduates demanded by industry. EUROPRACTICE provides European SMEs and start-ups with a true one-stop shop that provides all you need to design and fabricate electronic devices and systems in a supported cost-effective way with clear routes to prototype fabrication, commercialization and volume production.

- **Design Tool & Training website** europractice.stfc.ac.uk with the latest information related to EUROPRACTICE membership, purchase of design tool licenses, upcoming training courses and webinars;
- **Technology & Fabrication website** europractice-ic.com with detailed information on the MPW offer, run schedules, and pricing.

SOCIAL MEDIA

We are happy to see that our EUROPRACTICE community on LinkedIn and YouTube is growing. Following our accounts is a great way to stay informed about the latest service portfolio additions and share your experience with EUROPRACTICE.

On LinkedIn, we do not just publish announcements of new technologies and services, but we also give visibility to our customers by publishing their testimonials and technical user stories. At the beginning of 2023, our LinkedIn community counted more than 2500 followers.

The YouTube channel EUROPRACTICE Services gives a great opportunity to watch our webinar recordings. In February 2023, the channel had nearly 50000 views and almost 1000 subscribers, doubling the previous year's numbers.

CONFERENCES AND EXHIBITIONS

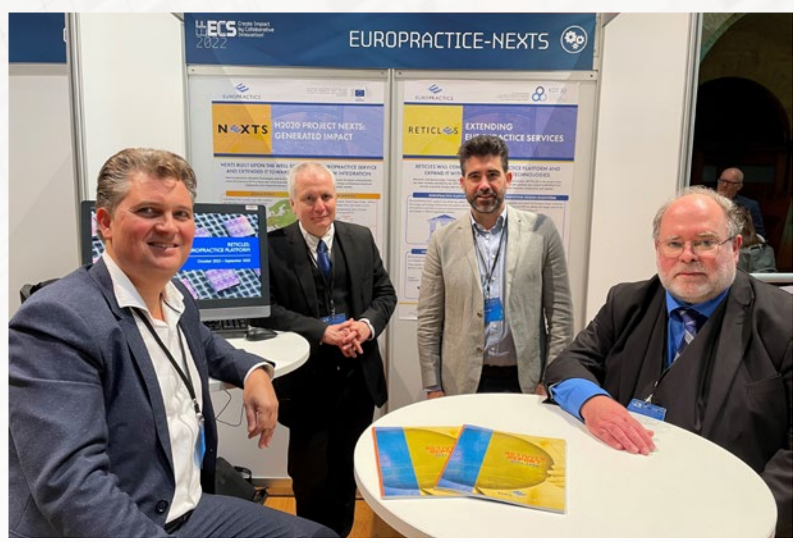
Every year, the EUROPRACTICE team is present at various scientific conferences, industrial trade shows and fairs to present our services to existing customers and to attract new prospects. In the first months of 2022, most events still took place online, such as ISSCC2022 and DATE2022.

Later last year, we were delighted by the opportunity to return to physical events and finally meet our customers face-to-face. The offline events started for us with PRIME in June 2022 and then continued with ESSCIRC-ESSDERC and EFECS in autumn, to name a few.

For our physical exhibition booths, we have updated 11 technology flyers and created three roll-ups presenting EUROPRACTICE MPW services, design-tool offer, and training courses respectively – all of it staying true to our well-recognisable bright-colour palette.

In 2023, we will attend at least the following conferences and fairs:

EUROPRACTICE booth at ESSCIRC-ESSDERC 2022



EUROPRACTICE team at EFECS 2022

LinkedIn invitation to visit the EUROPRACTICE book display at ISSCC 2023

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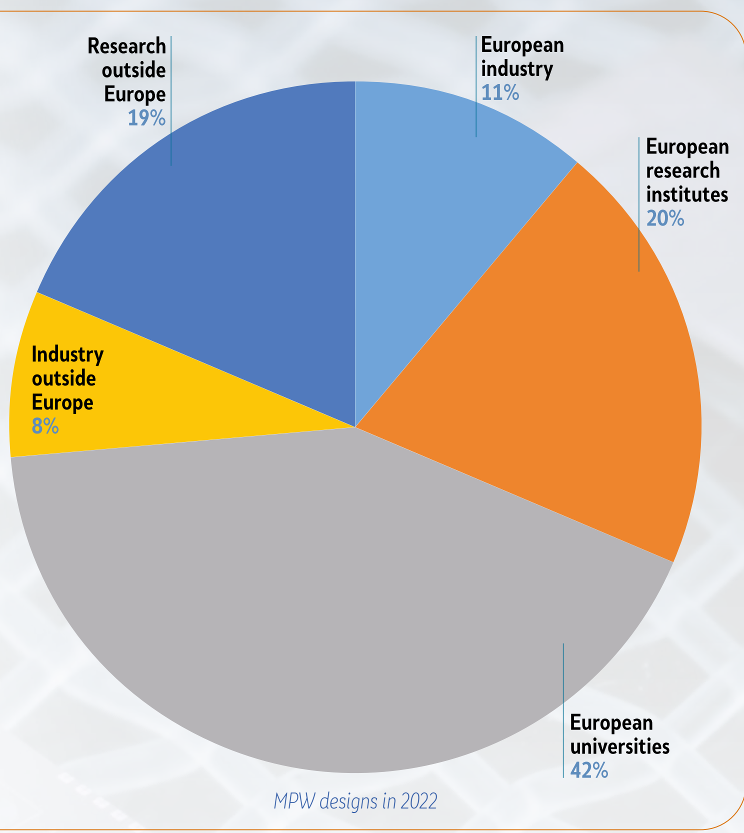
DATE 2023	Antwerp, Belgium	17-19 April
PRIME 2023	Valencia, Spain	18-21 June
SMACD 2023	Madeira Island, Portugal	3-5 July
ESSCIRC-ESSDERC 2023	Lisbon, Portugal	11-14 September
CadenceLIVE	Munich, Germany	TBD
ISSCC 2024	San Francisco, US	18-22 February (TBD)

RESULTS 2022: MPW PROTOTYPING SERVICES

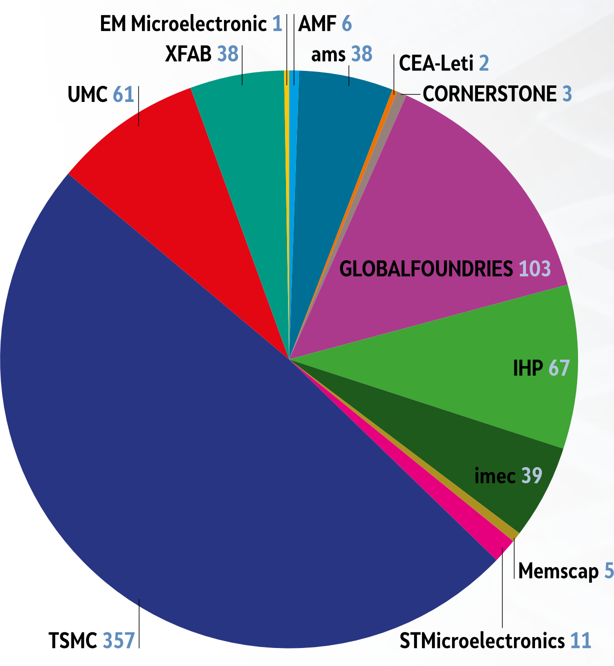
PROTOTYPED CIRCUITS ON MPW RUNS

For the first time in a decade, the number of prototyped designs on EUROPRACTICE MPW runs has declined. In 2022, 731 designs were submitted for fabrication compared to nearly one thousand prototypes the year before. Different factors can explain this. First of all, fabrication activities at very popular European foundries, including STMicroelectronics and ams, were temporarily stopped or limited due to administrative reasons. We also must mention the geopolitical tensions that led to the end of our relations with Russia.

Like previous years, European customers submitted most of the designs (73%), where 62% of the total submissions come from universities and research institutes and 11% from SMEs and startups.



MPW designs in 2022



Number of fabricated designs in 2022 per foundry

ACCESS TO TECHNOLOGIES OF WORLD-LEADING FOUNDRIES

Like previous years, most of the submitted designs in 2022 were fabricated in TSMC, the leading foundry for the global industry. It is followed by GlobalFoundries, which increased its numbers by nearly a third, and by a European R&D fab IHP, whose numbers have also shown good growth. The top two and three foundries of 2021 – STMicroelectronics and ams – had significantly decreased their shares of prototyped designs since their fabrication services were not available through EUROPRACTICE throughout the majority of 2022 due to administrative issues, which we hope to fix in the nearest future.

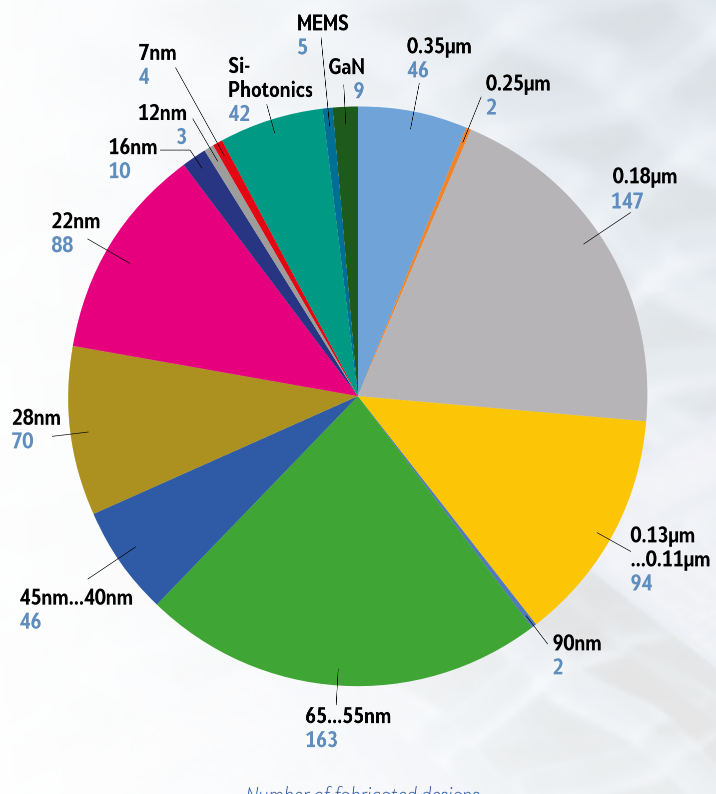
Among the highlights of 2022, we must mention the first three prototypes fabricated at CORNERSTONE, an open-source Si-Photonics foundry at the University of Southampton. They were submitted thanks to the design competition organised by EUROPRACTICE and CORNERSTONE.

GOOD TECHNOLOGY MIX

EUROPRACTICE offers a good technology mix. As you can see on the pie chart, advanced technologies, older technology nodes and More-than-Moore technologies are all used in significant volume.

The older technology nodes (ranging from 0.11µm to 0.35µm) are still very popular and represent approximately 40% of the submitted designs. For more advanced nodes, 65nm and associated nodes are the most popular, with 163 fabricated prototypes. Despite the temporary halt in the ST28FDSOI offer, we are pleased to see that other advanced technologies have kept increasing their popularity among EUROPRACTICE users. The number of designs in the 22nm FDSOI technology of GlobalFoundries has increased from 50 in 2021 to 88 last year. In addition, the share of prototypes in FinFET technologies of TSMC and GlobalFoundries with nodes ranging from 16 to 7 nm remains at a good level and slowly rises.

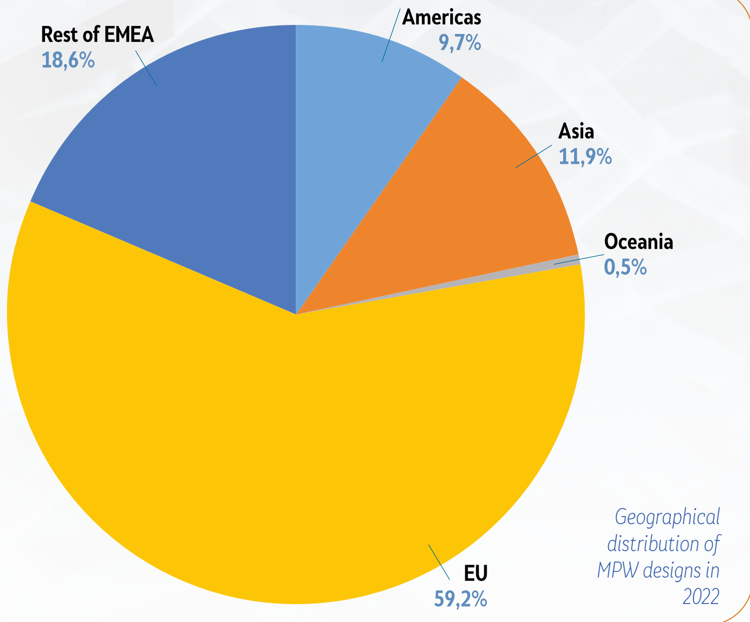
Finally, the number of submitted designs in More-than-Moore technologies, such as Si-Photonics, MEMS, and GaN-IC, remains at a good stable level.



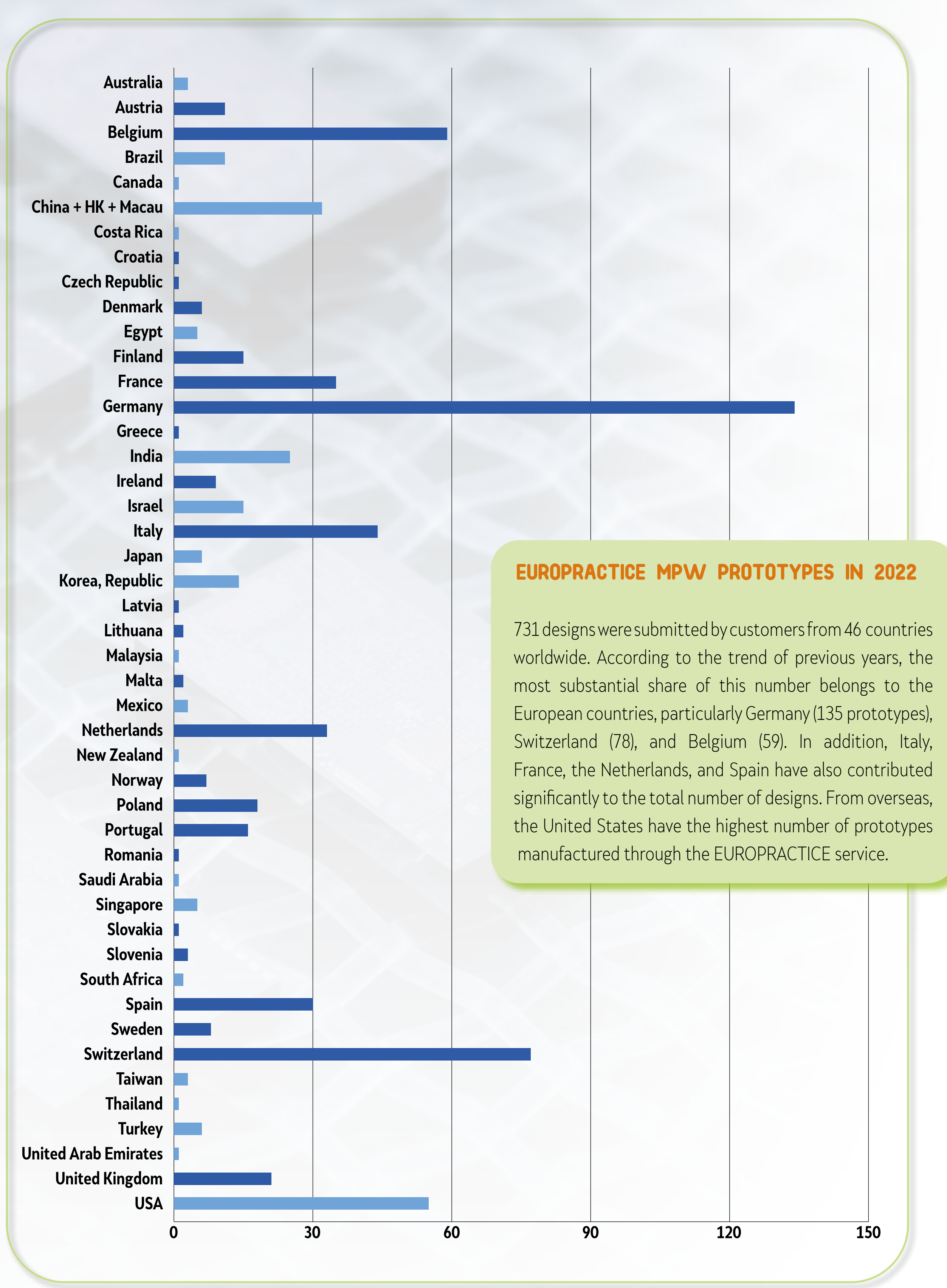
Number of fabricated designs in 2022 per technology (node)

GEOGRAPHICAL DISTRIBUTION

Continuing the trend of the previous years, more than three-quarters of the fabricated designs in 2022 come from Europe and the EMEA (Europe, Middle East and Africa) zone, where the total share of EU designs has slightly increased by 5% compared to 2021. A moderate number of customers from Asia also used the EUROPRACTICE prototyping services last year, representing a total volume of 87 designs. Finally, the remaining 10% of the manufactured prototypes are coming from the Americas and Oceania.



Geographical distribution of MPW designs in 2022



EUROPRACTICE MPW PROTOTYPES IN 2022

731 designs were submitted by customers from 46 countries worldwide. According to the trend of previous years, the most substantial share of this number belongs to the European countries, particularly Germany (135 prototypes), Switzerland (78), and Belgium (59). In addition, Italy, France, the Netherlands, and Spain have also contributed significantly to the total number of designs. From overseas, the United States have the highest number of prototypes manufactured through the EUROPRACTICE service.

USER STORIES ON PROTOTYPED DESIGNS

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Digital baseband controller for ZigBee applications

Phelma, Grenoble INP, Grenoble, France

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E-mails:	laurent.fesquet@univ-grenoble-alpes.fr, michele.portolan@univ-grenoble-alpes.fr

Technology:	ams 0.35µm CMOS C35B4 ISR15
Die size:	2mm x 2mm
Application Area:	Education

Introduction

As part of the Master of Microelectronics and Telecommunications (MT) at Grenoble INP / Phelma, an engineering school in Physics, Electronics and Materials, second-year students (equivalent to Master 1) worked on a project for designing a digital baseband controller for the ZigBee standard during their second semester. They faced situations very close to those they will experience in an industrial environment since the design of a chip requires not only designing the circuit but also carrying out numerous verifications guaranteeing the manufacturability of the integrated circuit. These verifications are mandatory steps before tapeout but are rarely carried out at school. Indeed, these verification steps are extremely time-consuming and require perseverance and tenacity. Finally, the circuit has been sent via the CIME-P services for fabrication in the technology ams C35B4.

Description

The circuit is a digital baseband controller compliant with the ZigBee standard. It has been split into several sub-blocks (Rx/Tx interfaces, IQ demodulation, image rejection filter, CORDIC / phase recovery, Clock-Data Recovery, block-wrapper) in order to share the design between students. This also makes it possible to test the blocks individually or connected, thanks to a block-wrapper.

Results

The circuit has been received in January and has yet to be tested.

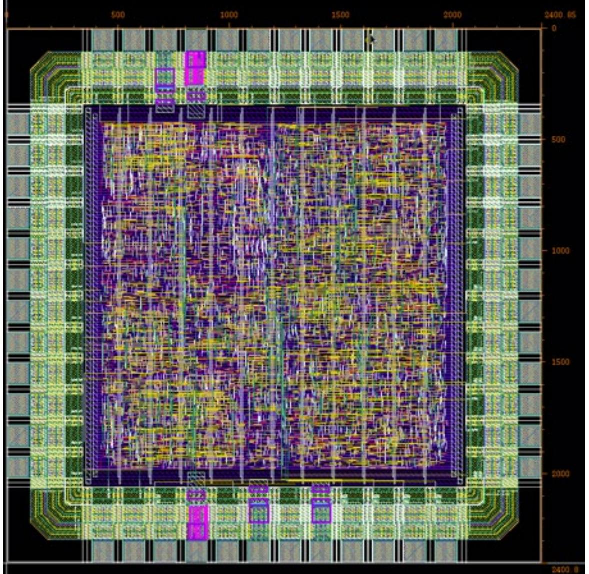

Fig.1: Layout of the circuit.

Why EUROPRACTICE?

Grenoble INP / Phelma has used the CIME-P services (previously CMP) for many years because they offer a cheap, simple and available technology suitable for Master students. Moreover, the number of runs per year is sufficient to guarantee that a tapeout slot will fit the academic year and the student agenda. Indeed, the circuit is designed during the second semester of the Master 1 and is tested during the second semester of the Master 2.

Acknowledgements

The students thank their professors (Laurent Fesquet and Michele Portolan) and the CIME-P team (Nicolas Partenza, François Bertholet, Kholdoun Torki, Isabelle Amielh, Abdelhamid Aitoumeri and Mohamed Ben Jrad) for their support during the design, DRC and LVS steps for finalising the chip layout.

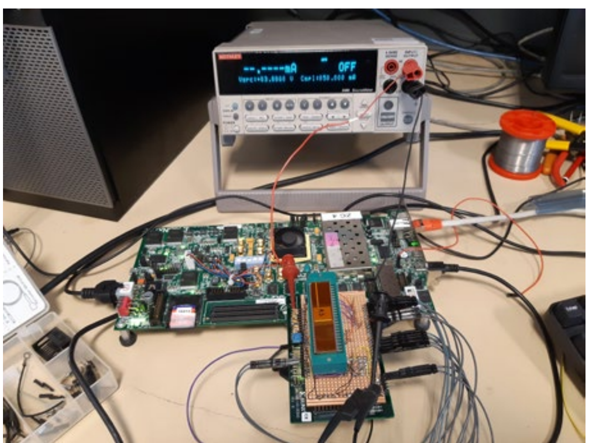

Fig.2: Testing the circuit.

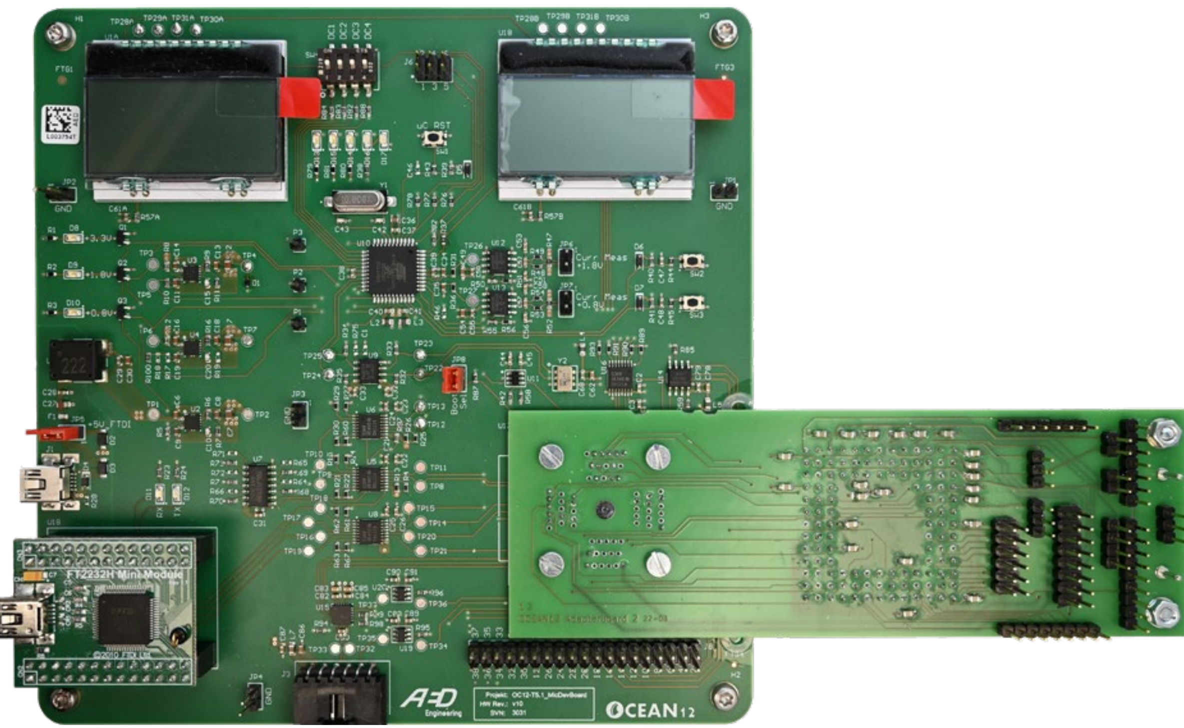

Fig.1: Development board.

An Ultra-Low Power RISC-V SoC with UltraTrail Accelerators for Speech Processing

Embedded Systems, University of Tübingen, Tübingen, Germany

Contacts:	Adrian Frischknecht, Paul Palomero Bernardo, Patrick Schmid
E-mail:	Adrian.frischknecht@uni-tuebingen.de
Technology:	GlobalFoundries 22nm FD-SOI 22FDX
Die Size:	1.25mm x 2.5mm
Design Tools:	Cadence
Application Area:	AI

Introduction

To reduce the dependency on the cloud for modern deep learning approaches, it is necessary to have performant and energy-efficient edge AI solutions. This also increases the availability, security, and privacy of the users. We achieve this by dedicated hardware accelerators for deep neural networks.

Description

For efficient on-device speech processing, such as voice activity detection and keyword spotting, we have designed dedicated specialized hardware accelerators and integrated them into a RISC-V SoC. The SoC is based on PULPissimo from ETH Zürich but is using a TGC RISC-V core by MINRES Technology which provides a better PPA for our use case.

Three hardware accelerators are integrated into the SoC to perform an FFT for feature extraction of the audio stream, and two UltraTrail 1D convolutional neural network accelerators. These UltraTrail accelerators have different sizes of memory and compute power as they are tailored for different applications. The first of the two detects if there is a human voice in the preprocessed audio stream. After successful detection, the second accelerator finds out if a predefined keyword is said. Depending on the result the SoC can execute a programmed action. Some idle modules like the SoC's memory and parts of the second UltraTrial instance can be turned into a low-power mode by power gating them when no voice is detected. Various power gating strategies can be applied by the programmed power management controller. Support for reverse body biasing was implemented to further reduce power consumption.
Additional to the SoC a completely separated large UltraTrail instance has been integrated to perform independent measurements and classifications without the SoC. This instance is quite large to support many different applications and to increase the performance by a multiple compared to the SoC's accelerators.

Results

The final chip just arrived but the first results show the functionality of the SoC and a successful switch from a QFP to a PGA package. Additionally, a strongly reduced power consumption compared to previous versions of the system is observed.

Why EUROPRACTICE?

Only with the affordable mini@sic multi-project wafer run by EUROPRACTICE for GlobalFoundries' 22FDX technology it was possible to gather experience for more complex designs and conduct our research. Furthermore, we appreciate the support during the design phase and the management of the packaging.

Acknowledgements

This work was supported through OCEAN12 (Grant Nr 783127) project, receiving funding from H2020 ECSEL JU program and German Bundesministerium für Bildung und Forschung (BMBF).

References

[1] Bernardo, P. P., Gerum, C., Frischknecht, A., Lübeck, K., & Bringmann, O. (2020). Ultratrail: A configurable ultralow-power tc-resnet ai accelerator for efficient keyword spotting. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 39(11), 4240-4251.

[2] Gerum, C., Frischknecht, A., Hald, T., Bernardo, P. P., Lübeck, K., & Bringmann, O. (2022). Hardware Accelerator and Neural Network Co-Optimization for Ultra-Low-Power Audio Processing Devices. arXiv preprint arXiv:2209.03807.

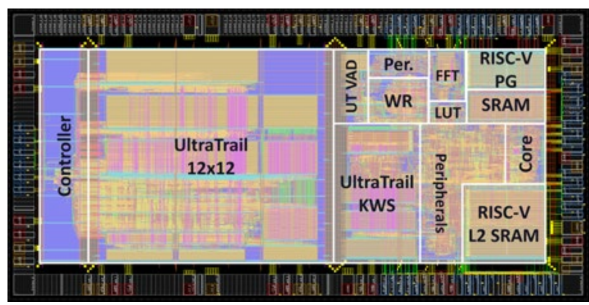

Fig.2: Layout of the circuit.

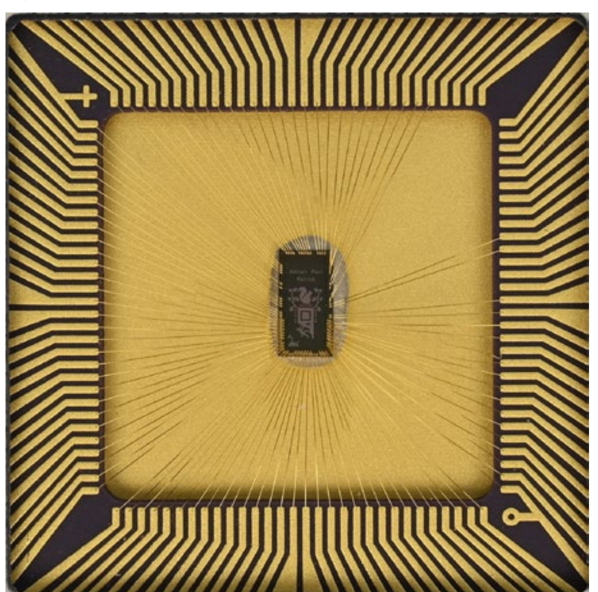

Fig.3: Photograph of the packaged die.

The Design of Functional Blocks of Transceiver for RF Sensing Applications

Institut für Mikroelektronik und Schaltungstechnik (EIT-4), Universität der Bundeswehr München, Neubiberg, Germany

Contacts: MSc. Rama Narayanan, MSc. Piyush Kumar, Dipl.-Ing Dario Stajic, Prof. Dr. Linus Maurer

E-mails: rama.narayanan@unibw.de; piyush.kumar@emft.fraunhofer.de; dario.stajic@unibw.de; linus.maurer@unibw.de

Technology: GlobalFoundries 22nm FD-SOI 22FDX

Die Size: 1mm x 1mm

Design Tools: Cadence IC Advance; Siemens Calibre (DRC, LVS, and XACT checks); ADS Momentum (EM Simulation of the coils)

Application Area: IoT

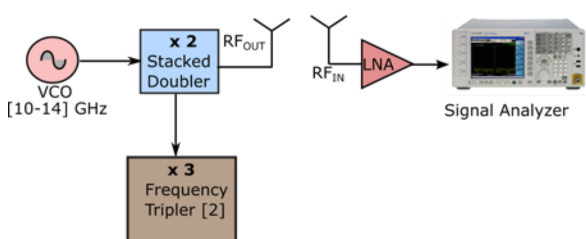

Fig.1: Block diagram of the proposed implementation.

Introduction

The evolution of modern-day Wireless Communication systems has ushered the research and development of 5G and 6G spectrums targeting different applications. Of course, moving higher into the radio spectrum offers numerous advantages, e.g., higher bandwidth, remote sensing and security.

Additionally, the advancement in lower node CMOS, e.g., 22nm FDSOI has augmented the feasibility of ultra-low power RFICs.

The main objective is as follows:

1. Design of low-power functional blocks of a sub 26 GHz transceiver for RF sensing applications, i.e., a Cross-coupled VCO with buffer and a stand-alone LNA.
2. Investigate various approaches for frequency-generation over a wide spectrum range suitable for different sets of applications (Beyond 5, IOTs, 6G, sensing), e.g., sub 26 GHz, 26-80 GHz.

Description

The cross-coupled VCO [1] contains two resonators: primary and secondary resonators. The inductors comprising the resonators of the proposed VCO are upgraded to a newer metal stack dedicated to RF and mm-Wave applications. The primary coil (Top) has one thick metal, whereas the secondary coil (Tail) has two stacked layers of Copper metals. Also, the tail resonator facilitates second harmonic rejection.

The VCO has a central frequency of 13 GHz and operates from 10 to 14 GHz at a 400mV minimal power supply. The VCO signal is upconverted using a stack-based frequency doubler and finally fed to a transmit antenna. A 26 GHz LNA at the receiver side should detect the transmit signals, and the output is visible employing a Signal Analyzer. Additionally, the frequency-doubled signal could be further interfaced with a frequency tripler designed in [2] to achieve a wide-band signal generation for Radar Applications.

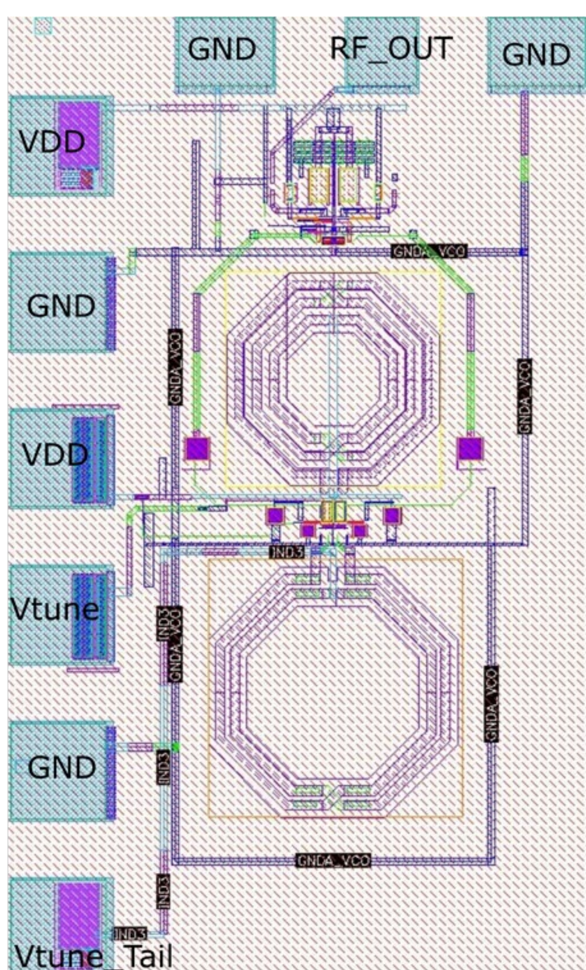

Fig.2: Chip layout of the proposed VCO with an output buffer.

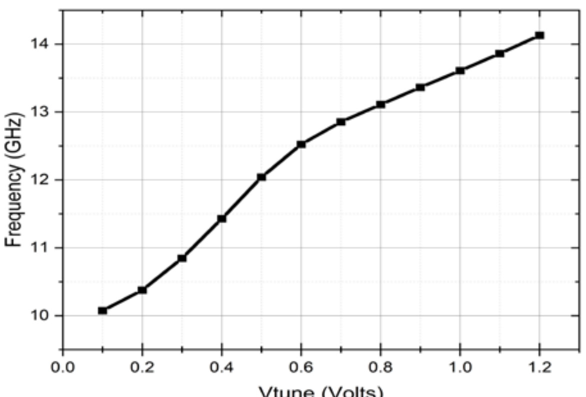

Fig.3: VCO's Frequency Tuning Response.

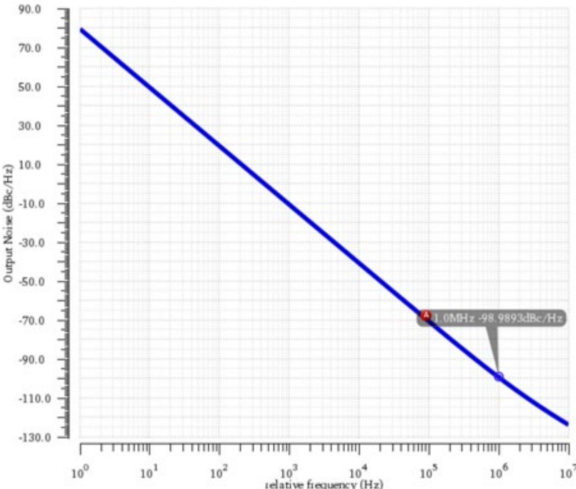

Fig.4: Simulated Phase noise @ 1MHz for a tuning voltage of 0.1 and frequency of 10 GHz.

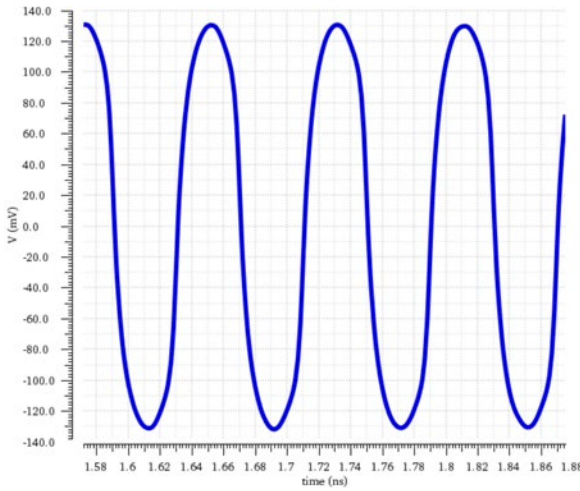

Fig.5: Transient Response for a tuning voltage of 600mV.

Results

VCO operates from 10-14 GHz for a varying tuning voltage from 0.1 to 1.2 V. The average output power and the average Phase noise delivered are -12.7 dBm and -92.15 dBc/ Hz @ 1 MHz, respectively. At the frequency of 10 GHz the lowest phase noise of -98.9 dBc/Hz @ 1 MHz offset is simulated.

Why EUROPRACTICE?

With EUROPRACTICE, our university had a successful series of tapeouts over the past several years with which we were able to develop various novel ideas and prototypes. This year our university participated in the mini@sic October 2022 tapeout in GF 22FDX technology for the OCEAN12 project.

EUROPRACTICE aims at providing the state of the art technologies with dedicated CAD tools licences, and PDKs at affordable prices. Hence as a researcher, we are always able to defend our proof of concept with Silicon validation. They always strive to provide Excellent support and cooperation during pre and post-tape out.

Acknowledgements

This work was supported through OCEAN12 (Grant Nr 783127) the project, receiving funding from the H2020 ECSEL JU program and German Bundesministerium fur Bildung und Forschung (BMBF).

References

[1] P. Kumar et al., "A 400 mV, widest-tuning-band- VCO with a central Frequency of 10.5 GHz and FTR of 2.5 GHz, designed in 22 nm FDSOI CMOS technology," 2019 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EURO-SOI-ULIS), Grenoble, France, 2019, pp. 1-4, doi: 10.1109/EUROSOI-ULIS45800.2019.9041894.

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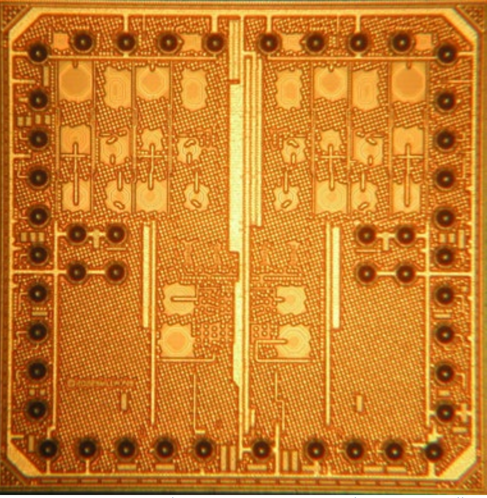

Fig.1: 5G Transceiver chip 1.25mm x 1.25mm, showing Cu-pillar.

5G Transceiver for mmW Digital beam forming

BeammWave AB, Lund, Sweden

Contact: Per-Olof Brandt
E-mail: Per-Olof@beammwave.com
Technology: GlobalFoundries 22nm FD-SOI 22FDX
Die Size: 1.25mm x1.25mm
Design Tools: Cadence
Application Area: Datacom / Telecom

Introduction

This RFIC is a prototype Transceiver to be used in BeammWave AB:s Digital Beamforming system solution. It covers multi band and dual polarization for the bands 24.25-29.5GHz (n258 and n257/261) and 37-40 GHz (n260).

Description

The design is highly integrated and integrates BB LP filters, PLL with 23bit resolution and VCO, Lo-generation, Tx-chain and PA, RX-chain and LNA. On chip voltage reference, LDO:s and digital control interface. The chip uses Cu-pillar bumping technology from GlobalFoundries.

Results

Using a multiple number of Tranceiver designs together, we are demonstrating the benefits with Digital beamforming for user equipment and smaller base station applications.

Why EUROPRACTICE?

The EUROPRACTICE consortium member Fraunhofer is the channel partner for GlobalFoundries. We had a great cooperation with Fraunhofer reaching the tapeout on time.

Acknowledgements

This work was supported by Cadence and GlobalFoundries.

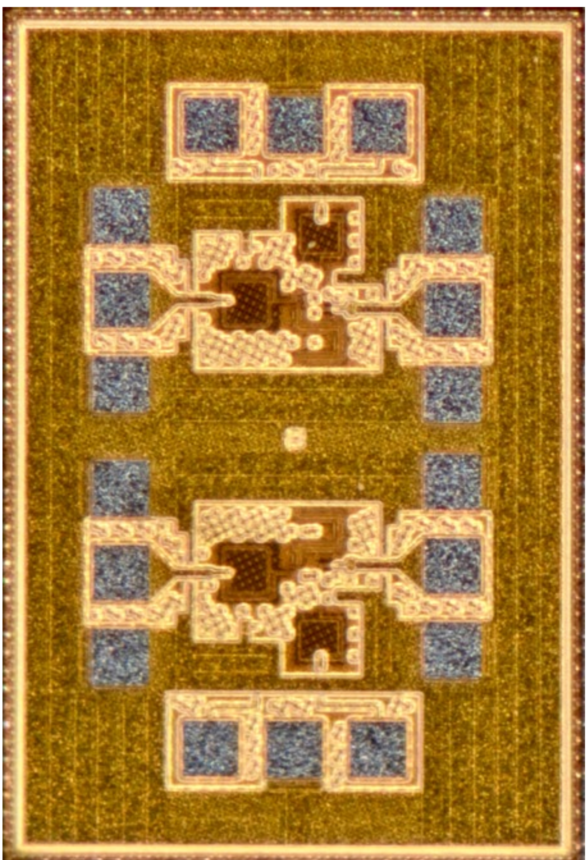

Fig.1: Microphotograph of the manufactured circuit.

GF-45RFSOI 25-GHz Cascode LNA

Institute for Applied Microelectronics (IUMA), Canary Islands, Spain

Contact:	David Galante Sempere
E-mail:	dgalante@iuma.ulpgc.es
Technology:	GlobalFoundries 45nm RFSOI
Die Size:	1.5mm x 1mm
Design Tools:	Cadence Virtuoso
Application Area:	Datacom / Telecom

Introduction

The LNA operates in the K-band, and is suitable for 5G New Release communications at mmWave frequencies. We carried out the design of this Low-Noise Amplifier as part of the GlobalFoundries University Partner Program because GlobalFoundries was interested in testing the performance of a particular device, which was originally intended for PAs, in a low-power cascode LNA operating at a central frequency of ~25 GHz. GF is interested in measuring the noise performance of the device in this context.

Description

A low-power 25-GHz cascode LNA has been designed. Two versions of the LNA were sent to the foundry, so that the performance of two different layouts of the common-source transistor can be tested.

Results

The first-round version of the LNA achieves a NF of 1.6 dB with a total gain of 14 dB, Input and Output Return Losses better than 10 and 6 dB, respectively, and I/O Isolation of 20 dB at a frequency of 25 GHz. The circuit draws a total current of 11 mA from a 0.9 V DC power supply and occupies an area of 0.7 mm x 1 mm including pads and guardring. At the moment we are waiting for the arrival of the second-round prototypes to perform the measurements.

Why EUROPRACTICE?

We used EUROPRACTICE Services because they offer access to cutting-edge technologies and provide support for tapeout procedures for GDSII submission. Likewise, EUROPRACTICE provides prototyping, packaging and testing services for state-of-the-art technologies with mature PDKs at fair prices. Without these services, we would be unable to participate in a project of this magnitude.

Acknowledgements

This work has been partially supported by GlobalFoundries, by the Canarian Agency for Research, Innovation, and Information Society (ACIISI) of the Canary Islands Government by Grant TESIS2019010100 Grant PID2021-127712OB-C21 funded by MCIN/AEI/10.13039/501100011033, and by "ERDF a way of making Europe".

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Smart Sensors for Low Visible Lighting Conditions in Different Applications

ScReIn UG, Hamburg, Germany

Contact:	Andrey Saveliev
E-mail:	service@screin.eu
Technology:	GlobalFoundries 130nm BCDlite
Die Size:	7200µm x1250µm
Application Area:	Automotive / Transport

Introduction

Smart Digital Visual Sensors which are able to detect very low photon fluxes – down to single photons – may be used in various areas which either require very low radiation levels (as, for example, in experimental physics) or which are specifically designed to operate in low-light conditions in order to be able to measure even the slightest changes in intensity with excellent time response for various future applications, e.g. in the automotive sector.

Description

Silicon Photomultipliers (SiPMs) [1], developed by members of our organisation, are known to be the exceptional detectors for visible light, as they are able to detect photon fluxes down to single photons, therefore pushing the technology to the limits of what is physically possible. At present, there is no real alternative in this area. Based on this [2], we are developing the next generation of Smart Digital Visual Sensors for low photon fluxes which provide both a completely digital signal processing without the intermediate step of an analog-to-digital conversion and processing directly on the chip – a smart System-on-Chip. In order to realise that, i.e. combining the sensor and processing electronics on the chip, we are using modern semiconductor technologies, including CMOS processes.

Results

We have produced several generations of different versions of Smart Digital Visual Sensor prototypes for low photon fluxes with integrated processing electronics – a System-on-Chip based on the CMOS process. At present, we are working on the optimisation for different future applications, in particular in the automotive sector.

Why EUROPRACTICE?

The most promising progress for applications in different areas is based on modern semiconductor technologies. EUROPRACTICE provides a cost-effective possibility to develop a System-on-Chip for new Smart Digital Sensor Systems even for innovative small-scale companies and a flexible and fast transfer to the industrial production of sensor components for various smart visualisation systems. Also, since we started in the field, EUROPRACTICE provided valuable help with organisational and technical issues on the way to a tapeout and also with the chip design, such that we were able to gain important experience with that as well for future developments.

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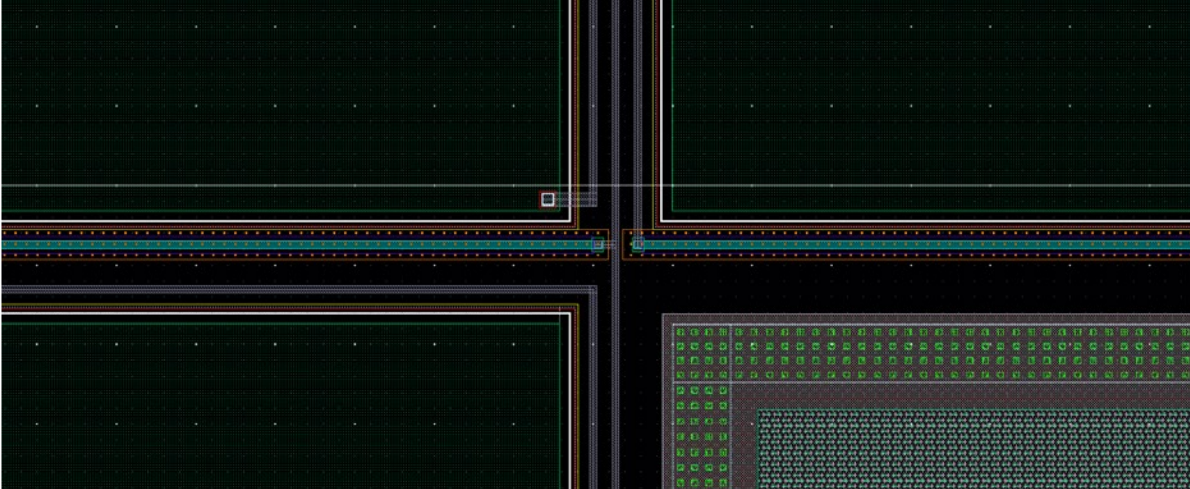

Fig.1: Detailed view of the sensor part of the Smart Digital Visual Sensor.

Compressive Sensing Ultra-Wideband Receiver Frontend Chipset: XG1 + XF1

Technische Universität Ilmenau, Fraunhofer IIS, Germany

Contacts:	Christoph W. Wagner, Kevin Drenkhahn
E-mails:	Christoph.wagner@tu-ilmenau.de, kevin.etienne.drenkhahn@iis.fraunhofer.de

Technology:	IHP 0.13µm SiGe BiCMOS SG13S
Die Size:	1000µm x 800µm (both devices)
Design Tools:	Cadence Virtuoso, Maestro, Assura, Genus, Innovus
Application Area:	Ultra-Wideband Signal Acquisition Radar, Channel Sounding and Parameter Estimation

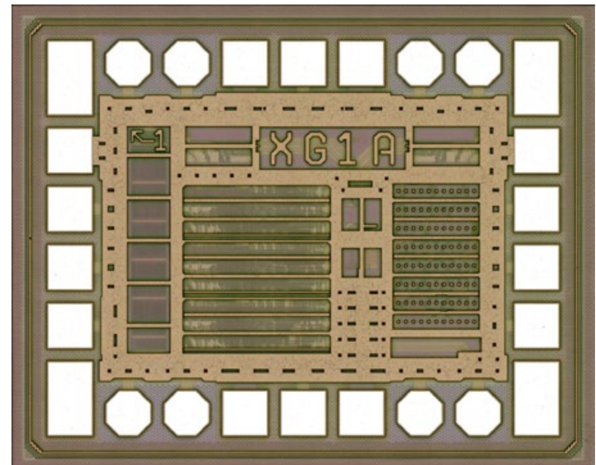

Fig.1: Die-Shot of the "Xampling Generator" XG1 integrated device.

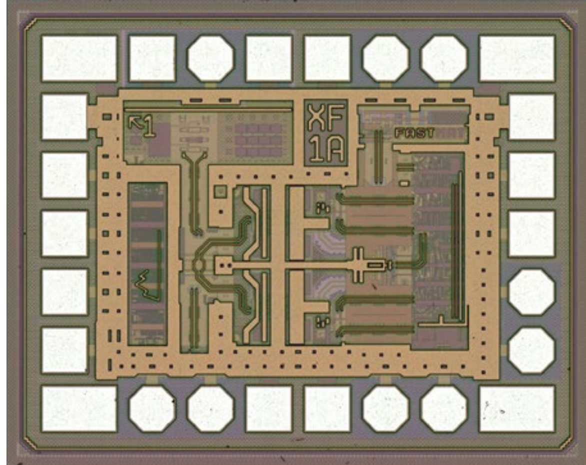

Fig.2: Die-Shot of the "Xampling Frontend" XF1A integrated device.

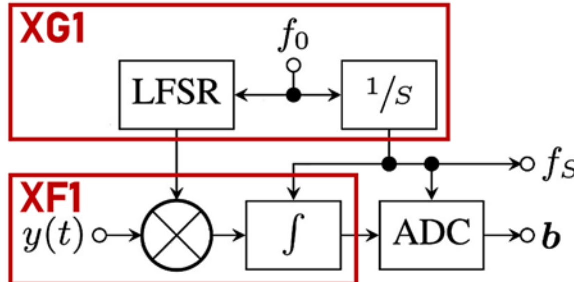

Fig.3: Block Diagram of a Compressive Sensing Receiver and its mapping to device functions of the chipset.

Introduction

Compressive Sensing (CS) is a signal acquisition concept, enabling the perception of signal properties from only a few observations, that are taken well below the Nyquist-Rate associated to the spectral shape of the signal. This trickery is possible as long as there exists some signal space (like an algebraic basis), where the signal can be described from only a few non-zero components in that base. Further, a linear combination with a deterministic pseudo-random (PR) mixing signal must be performed in the analog domain, prior to digital conversion, to achieve compression.

Typical hardware architectures include the Random Demodulator (RD) or Modulated Wideband Converter (MWC). However, for demanding applications such as ultra-wideband radar or beam-finding in massive-MIMO satellite communications, available devices as well as contemporary system- or circuit topologies generally lack the required flexibility and support for high-frequency operation.

Description

We have designed a chipset, consisting of two integrated circuits, which together form a CS-receiver for signal frequencies up to 30 GHz, an instantaneous bandwidth of up to 15 GHz and output sampling rates ranging from 10 to 250 MSps:

The XG1 – "Xampling Generator 1" device implements a fully-configurable linear feedback shift register (LFSR) of arbitrary order up to 24 for the purpose of generating PR-mixing signals, and a reconfigurable integer-N clock divider, capable of arbitrary division factors of 8...1048583 for providing timing control of the linear combination windows. Both generated signals can be fully synchronized to an external clock and event source, allowing for true multi-channel operation of many devices. The XG1 device is also well-suited for implementing pulse-compression radar systems based on the m-Sequence method. High-speed logic is implemented in specialised logic cells featuring dynamic power-shut-off by combining PECL logic

paths with combinatorial CMOS "enable"-paths for switching not-needed logic paths dark during operation. This results in a severe reduction of power consumption, depending on the chosen device configuration. Please check out the provided references for more details on the internal mode of operation or performance figures.

The XF1 – "Xampling Frontend 1" device implements an analog engine for forming piecewise-continuous linear combinations of the input RF-signal in the analog domain. After an LNA input stage, that supports RF-signal frequencies from 1 MHz up to 30 GHz, a Gilbert-cell applies sign-inversion to the input signal, corresponding to the PR-mixing signal generated by the XG1 device. Finally, the resulting signal is integrated to complete the analog linear combination using the timing-control (clock) signal, generated from the XG1 divider. Operating two identical integrator cores in an alternating ping-pong fashion allows for continuous operation with full back-to-back integration. An output multiplexer warrants that the corresponding hold-phases can be delivered to the output while the other integrator still is active, integrating the following observation sample without interference or "missed spots".

Both circuits operate from a single 2.5 V supply and feature an on-chip 1.25 V linear regulator for CMOS logic, full ESD-protection on all pins (including RF) and an integrated I2C bus device core for reconfiguration purposes and tuning of analog biasing circuits. On top, an individual bus address can be assigned to each device for operating many circuits on a single I2C bus.

Results

Both devices were shown to operate functionally correct under laboratory conditions. The XG1 device proved its capability to correctly and reliably generate arbitrary shift register sequences and clocks, regardless of chosen configuration. Furthermore, four XG1 devices were also shown to accurately align to an external clock and synchronisation signal, generated from a JESD-204B clock source running at 7 GHz, with an overall output timing mismatch of only +/-10 ps. Measured power consumption of each XF1 device is 0.7 Watts and ranges from 0.3 to 0.9 Watts for any XG1 device (depending on configuration). Ongoing work includes the characterisation of the XF1 devices' analog performance, calibration of the frontend for compressive-sensing sparse-signal-recovery (SSR), and the in-system test of multiple XG1/XF1 devices in a four-channel CS-receiver demonstrator.

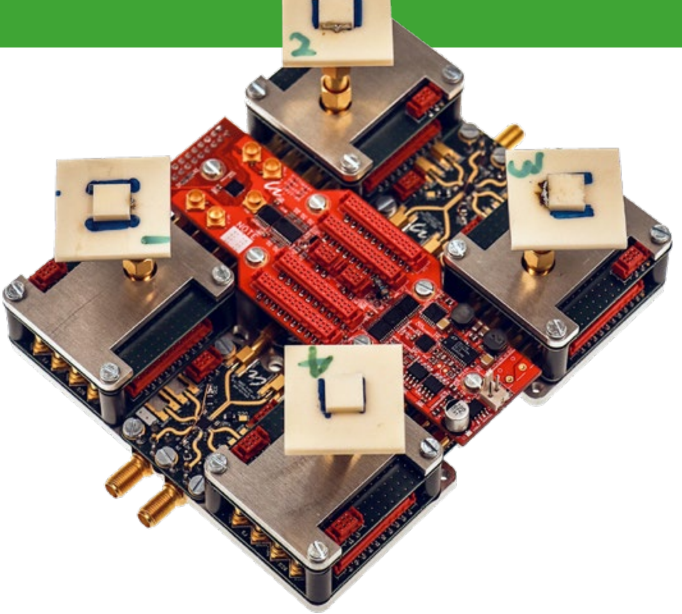

Fig.4: The four-channel Lab-Demonstrator featuring four XG1- and four XF1 devices, configured for time-domain beam-search in satellite-communication or multi-channel compressive-sensing ultra-wideband radar applications.

Why EUROPRACTICE?

EUROPRACTICE provides essential services and access to relevant resources that enable research institutions to design, produce and package their custom integrated-circuit designs, ultimately fuelling fundamental and application-oriented research. We were very happy with the support received and are grateful for the economically very viable conditions offered through the MPW program. In addition, EUROPRACTICE allows us to fabricate small, single use case circuits for testing and preparation of future larger scale developments. This would otherwise not be possible due to the high entry costs of integrated circuit design.

Acknowledgements

The designers would like to express thanks to the Carl-Zeiss-Foundation for supporting this work, carried out in the PRIME research group at the Technische Universität Ilmenau and the research group of Gerald Kell at the Technische Hochschule Brandenburg for the Common-ECL digital library from the BMBF-project EuRISCOSi.

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24-31 GHz Power Amplifiers (basic, balanced and Doherty) for 5G applications

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Contact:	Gwennaël Diverrez
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Technology:	ST 28nm FD-SOI CMOS
Die Size:	1450µm x 1450µm
Application Area:	Datacom / Telecom

Introduction

We have created these circuits in order to meet the expectations of 5G, i.e. performance in efficiency with a back-off in power while maintaining robustness to 3:1 VSWR variations in the framework of a thesis. Indeed, 5G base stations as well as user equipment require a lower power consumption than 4G ones and the power amplifier is the main energy consuming component in RF transceivers. Therefore, high challenges on efficiency are proposed to limit their effect. In addition, the Doherty architecture is inherently narrowband. The objective of this thesis and of this circuit is to propose a solution to extend the theoretical bandwidth of the Doherty architecture.

Description

Three architectures have been designed to meet these expectations: a basic power amplifier, a balanced amplifier and a Doherty amplifier. The most interesting architecture of the three presented is an innovative Doherty power amplifier topology using a hybrid coupler-based architecture. Thanks to its hybrid coupler-based structure, the amplifier is able to present high efficiency with power back-off over a wide bandwidth while presenting immunity to VSWR variations. Indeed, the hybrid couplers present theoretical wide band behaviors which allow to offer to the Doherty amplifier a wide band operation contrary to the traditional lambda/4 lines.

Results

All three amplifiers maintain state-of-the-art performance in the 24 - 31 GHz band. The elementary line shows maximum efficiency above 42% first. The balanced amplifier presents a state of the art efficiency performance for balanced amplifiers at 26 GHz (37%) while being robust to 3:1 VSWR variations. Finally, the Doherty amplifier presents high wideband efficiency performances at maximum power and with 6 dB of power back-off while being robust to VSWR variations of 3:1.

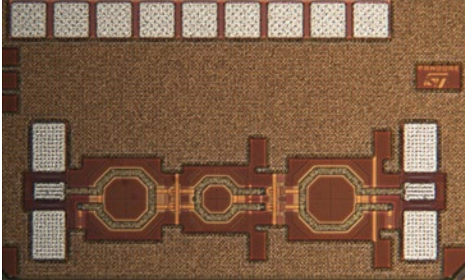

Fig.1: Picture of the basic amplifier.

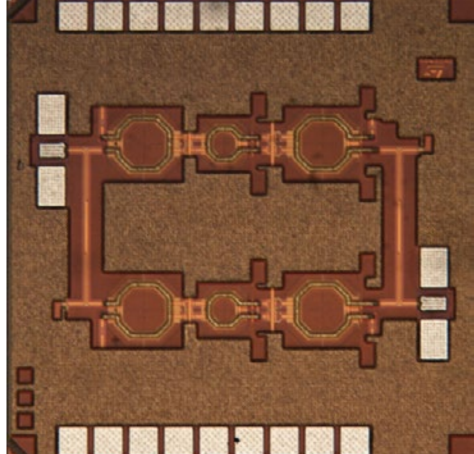

Fig.2: Picture of the balanced amplifier.

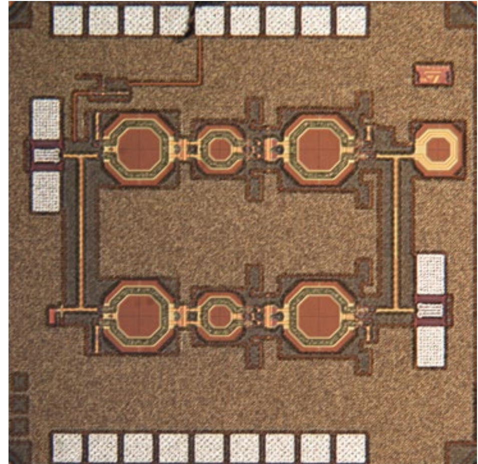

Fig.3: Picture of the Doherty amplifier.

Why EUROPRACTICE?

Within the framework of the joint ST-IMS laboratory in Bordeaux, my thesis work was supported by STMicroelectronics and the design of the circuits by CIME-P (former CMP).

Acknowledgements

We would like to thank STMicroelectronics for chip manufacturing and Rohde&Schwarz for measurements.

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Warm front-end for X-ray cryogenic detectors

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Technology:	ST 130nm BiCMOS9MW
Die Size:	2mm x 2.7mm
Application Area:	(Aero)Space

Introduction

AwaXe_v4 (Athena Warm Asic for the X-ifu Electronics - Version 4) is a technological demonstrator of the ST 130nm SiGe BiCMOS technology. It integrates the re-design of the analog parts to replace those already in an existing ASIC "AwaXe_v3" based on the ams 350 nm SiGe BiCMOS technology. This shift from ams to ST is required by the long-term development of a flight model ASIC for the Warm Front-End Electronics of the future X-ray observatory: ATHENA, a space mission of ESA.

The AwaXe_v4 includes a low-noise amplifier and adjustable, low-noise and low-drift biasing for superconducting devices (SQUID and TES). These components assure the analog functions of the warm (~300 K) front-end integrated into the Time-Division Multiplexing readout of the X-IFU instrument of the ATHENA observatory.

This ASIC belongs to the "AwaXe and SQmux ASIC families" developed at APC Laboratory for SQUID/TES readout.

Description

AwaXe_v4 is an ASIC including the analog functions of the WFEE, mainly composed of:

- Two quasi-identical fully-differential low-noise amplifiers (one with input offset compensation). The gain-bandwidth product is larger than 3 GHz (gain ≈ 160 V/V, bandwidth > 20 MHz). The intrinsic input noise is below 0.5 nV/√Hz even at room temperature, and is maintained below 1 nV/√Hz whatever the offset compensation. This voltage spectral density referred to the input includes voltage noise and current noise contribution via an input cryogenic (~noiseless) load up to 200 Ω. The sizing the LNA allows to keep 1/f noise corner frequency below 100 Hz. Non-linearity is better than 1% from DC until 9 MHz with 2 Vpp output amplitude. Gain drift stays below 300 ppm/K in the range of [17°C, 37°C]. Input and output impedance matching is also practicable;

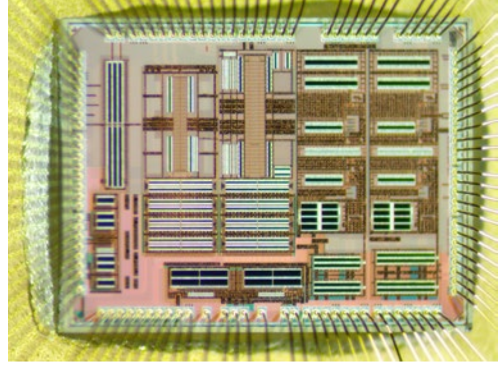

Fig.1: Microscopic photo of the ASIC "AwaXe_v4", 2mm x 2.7mm with pads

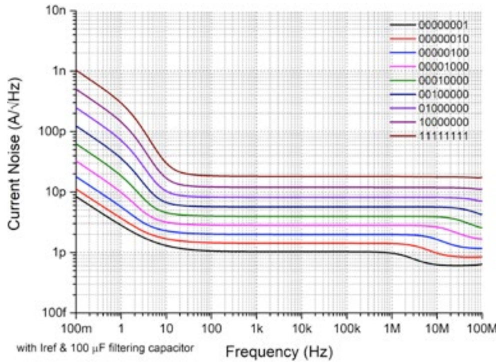

Fig.2: DAC noise results.

- A low-noise and low-thermal drift band-gap current reference with four outputs of 2.2 mA;
- Two quasi-DC 8-bit digital-to-analog converters (one of [0, 2.2 mA], the other of [0, 600 µA]), with differential outputs, ultra-low output current noise: 1/f noise corner frequency (<100 Hz) and white noise < 100 pA/√Hz, low INL and low thermal drift (< 100 ppm/K);
- An on-chip thermometer for sensitive housekeeping without common-mode coupling;
- Test devices (bipolar transistors, MOSFETs, MIM capacitor, resistor...) to characterise radiation dose effects and operations at both room and cryogenic temperatures.

Results

One of the interesting results is the output noise of the current DAC, of which the 1/f corner frequency is kept below 100 Hz and white noise is about 10 pA/√Hz.

Why EUROPRACTICE?

We benefit from the MPW EUROPRACTICE services via CIME-P (former CMP) in France. And we are waiting for a new run of the ST 130 nm SiGe technology to send our 3 already-designed ASICs.

Acknowledgements

The development is funded by ESA, CNES and CNRS.

References

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An 8.2-to-10.2 GHz ADPLL for Automotive Applications

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E-mail:	ias.rwth-aachen.de
Technology:	TSMC 28nm HPC+
Die Size:	1.413mm x 1.413mm
Design Tools:	Cadence Virtuoso, Spectre RF, Xcelium
Application Area:	Automotive / Transport

Introduction

With the fast advancing into IoT and 5G era, the phase noise performance and the channel selection ability of the local oscillator (LO) in a modern communication system face difficult challenges. In an electro-magnetic (EM) harsh environment such as automotive applications, having a robust and reliable LO is necessary. For such applications, the all-digital PLL (ADPLL) is currently drawing more attention as it is inherently less prone to environmental fluctuation such as supply voltage variations. The goal of the design is to achieve a comparable phase noise performance with a very fine frequency step.

Description

The design constitutes a low-phase noise and spur-free All-Digital Phase-Locked-Loop (ADPLL) operating from 8.2 to 10.2 GHz with a tuning step size in the range of tens of kHz. To achieve a robust and reliable operation in such environments, special care was taken during the design of the ADPLL to suppress and mitigate noise from power supply lines and external coupling. The analog components target state-of-the-art performance with a low-phase noise digitally controlled oscillator (DCO) and a time-to-digital converter (TDC) with a high resolution in the picosecond range. The digital signal processing core (DSP), which is configurable via SPI, allows switching PLL type and bandwidth settings. Additionally, the digital loop filter inside the DSP integrates a predictive spur cancelation algorithm to suppress fractional spurs. Special care was taken to shield the analog components from supply variation and coupling. Therefore, a high-accuracy bandgap and a low-noise low-dropout regulator (LDO) are used to provide separate supply

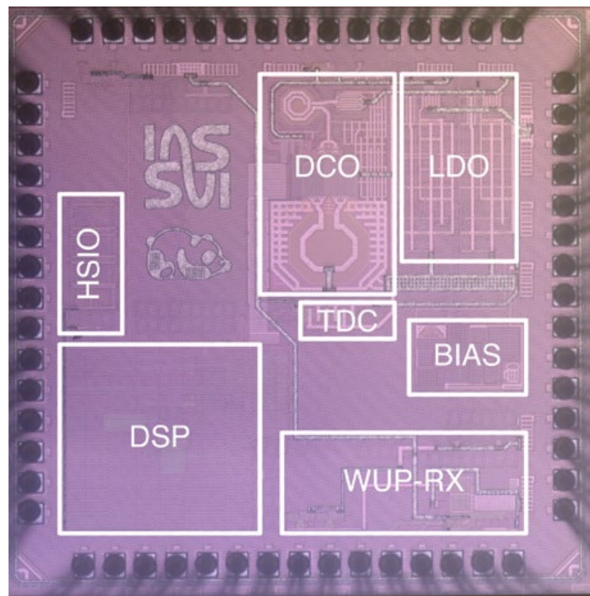

Fig.1: Chip micrograph.

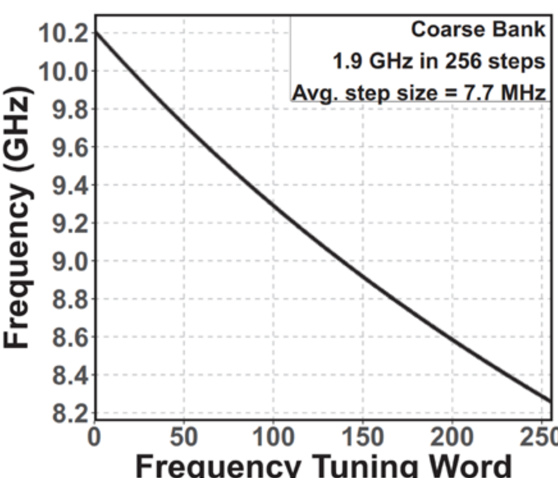

Fig.2: Measured tuning range of the free-running DCO.

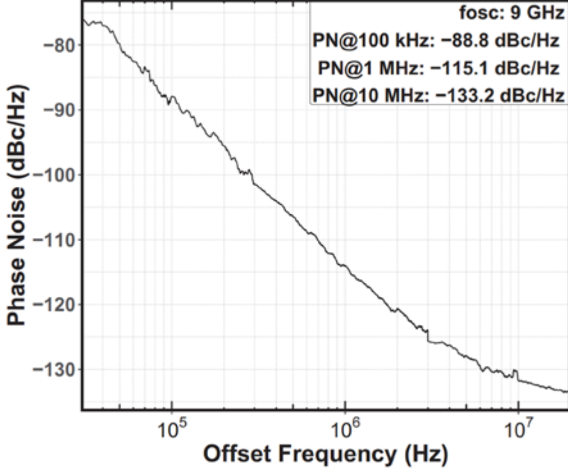

Fig.3. Measured phase noise of the DCO at 9 GHz.

domains for DCO, TDC, and DSP. The integrated high-speed high data rate interface (HSIO) allows bypassing the on-chip loop filter and investigating additional topologies using an external FPGA. The spare die area allowed us to additionally tapeout an experimental wake-up receiver (WUP-RX) for first in-silicon measurements beneficial for its further development.

Results

Figure 2 shows the measured frequency tuning range of the DCO of 8.2 to 10.2 GHz in 256 steps with a tuning step of 7.7 MHz. The measured phase noise of the free-running DCO is depicted in Figure 3. The design achieves a phase noise of -115.1 dBc/Hz at 1 MHz offset from 9 GHz carrier frequency. The measured performance aligns quite well with the simulated result using the extracted layout, which shows good accuracy of the model provided by TSMC via EUROPRACTICE.

Why EUROPRACTICE?

EUROPRACTICE's mini@sic program is an exceptional opportunity for university research groups to do affordable prototyping in state-of-the-art nanoscale semiconductor technologies. Obtaining access to key software IC design tools and foundry PDKs from one single partner greatly eases our design activities. The profound technical assistance as well as the customer-friendly attitude of its staff members is invaluable throughout the entire design process from PDK setup to final tape-out. Without EUROPRACTICE and their mini@sic program taping-out and evaluating, the outcomes of our research in-silicon would be virtually impossible, thus, it enhances our research activities significantly.

Acknowledgements

We would like to express our gratitude to EUROPRACTICE and imec for their excellent support during this tapeout and throughout the last years.

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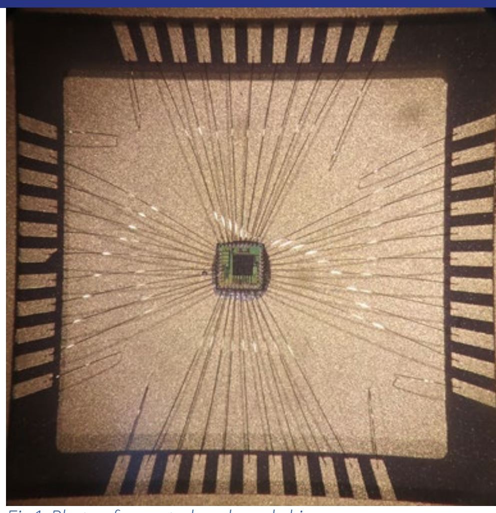

Fig.1: Photo of mounted packaged chip.

Prototype chip implementing indirect voltage measurement method using noise distribution measurement

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Technology:	TSMC 28nm HPC+
Die Size:	1mm x 1mm
Design Tools:	Cadence Virtuoso, Spectre, Genus, Innovus, Xcelium; Siemens Calibre
Application Area:	High Energy Physics (HEP)

Introduction

The designed IC prototype implements an indirect voltage measurement method, measuring and fitting the noise distribution curve [1]. The main target of this prototype is to adapt the method mentioned to a semiconductor pixelated X-ray detector, which should increase the accuracy of the event particle energy measurement based on the pulse amplitude measurement.

Description

The described chip consists of a 7x7 pixel matrix, bias circuits, analog multiplexer, and SPI interface. Each pixel in the matrix has implemented a charge-sensitive amplifier (CSA) with very slow signal slope at the output (after measurement the CSA is discharged) and 8 pairs of comparators, each connected to a 16-bit counter, which is required to implement the algorithm. Such a high number of comparators allows us to extend the dynamic range of the circuit, which depends on the CSA output noise and the required threshold range. As the noise in the circuit is (mostly) fixed, we can only increase the threshold levels 'pitch' and the number of comparators. Long counters allow to collect better statistics required for better Gauss curve fitting. Additionally, threshold

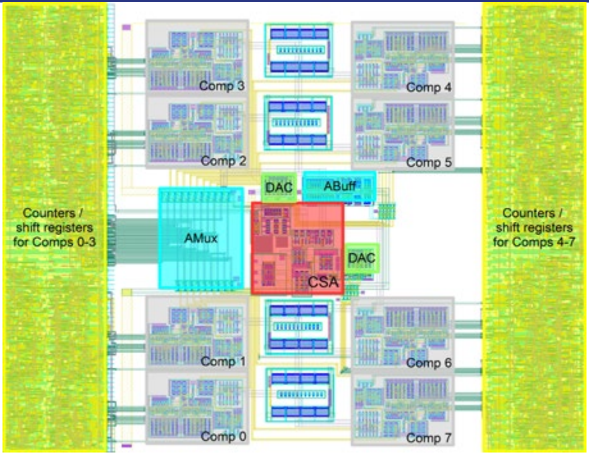

Fig.2: Pixel block diagram.

level trimming circuits allow working with combined correlated double sampling [2], where 4 comparators are used to measure the baseline noise distribution, and another 4 comparators measure the noise distribution in the signal. There are also high-precision DACs for mismatch compensations in pixels. The pixel size is 75µm × 75µm, although the scale-down is possible since there is a lot of free space within the pixel. Base debugging is done by the analogue multiplexer, which makes it possible to observe the DACs characteristics and circuit DC levels. Communication using the SPI interface provides access to configuration and matrix data using dedicated registers for clock and data in/out. As a prototype, the IC is not designed to be connected to any real detector, instead of that a simple calibration circuit is implemented to inject the charge to the input of the CSA in each pixel.

Results

Preliminary measurements show the proper functionality of pixel- and chip-level digital subsystems, which means a working SPI interface and chip-to-matrix communication. The analogue part is under investigation.

Why EUROPRACTICE?

EUROPRACTICE offers cost-efficient low-area IC prototyping (mini@sic) in a leading IC manufacturing company, which gives us the possibility to minimise costs and achieve the best possible performance. The high-quality packaging service also plays a role, when the time is very important.

Acknowledgements

The work was supported by the Polish Ministry of Science and Education under contract no. 0138/DIA/2020.

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A 12 Bit 8 GS/s Time-Interleaved PRBS-Scheduled SAR-ADC with On-Chip Calibration-Engine in TSMC 28nm HPC+

Chair of Mixed Signal Circuit Design, Technical University of Berlin, Germany

Contacts:	Sebastian Linnhoff, Frowin Buballa
E-mails:	Sebastian.linnhoff@tu-berlin.de, f.buballa@tu-berlin.de

Technology:	TSMC 28nm HPC+
Die Size:	3900µm x 2400µm
Application Area:	Datacom / Telecom

Introduction

One of the most important application fields for high speed analog-to-digital converters (ADCs) are the broadband communication sector, high accurate radar systems and instrumentation applications. Systems such as 5G & 6G mobile infrastructure and direct conversion radar systems e.g. in the field of self-driving automobiles are facing exponential increase in demand. These systems require the highest performance in terms of linearity and noise across their entire bandwidth. These challenges can only be tackled by innovative design approaches with a mix of high performance analog circuit design in combination with digital calibration techniques to overcome the performance gaps of 28nm analog circuits and reliably achieve 12 bit linearity.

Description

In this project a high speed 8 GS/s 18x randomly-scheduled time-interleaved 12 bit SAR-ADC is developed and fabricated. The design makes use of 16+2+1 parallel SAR-ADC lanes to enable an individual channel sample rate of 500 MS/s including channel randomisation and an additional reference SAR used for calibration. Each of 18 ADCs makes use of 14 conversion cycles, including capacitive redundancy, to achieve 12 bit resolution and an additional 2 conversion cycles for sampling. To be able to drive this circuit, a network of ultra-wideband input buffer is utilised. To achieve the targeted linearity of >70dBc at full scale input voltage, multiple pseudo differential class AB buffers are used. Each SAR is built from an ultra-fast loop-unrolled comparator, C2C-DAC structure as well as highly optimised finite state machine to implement

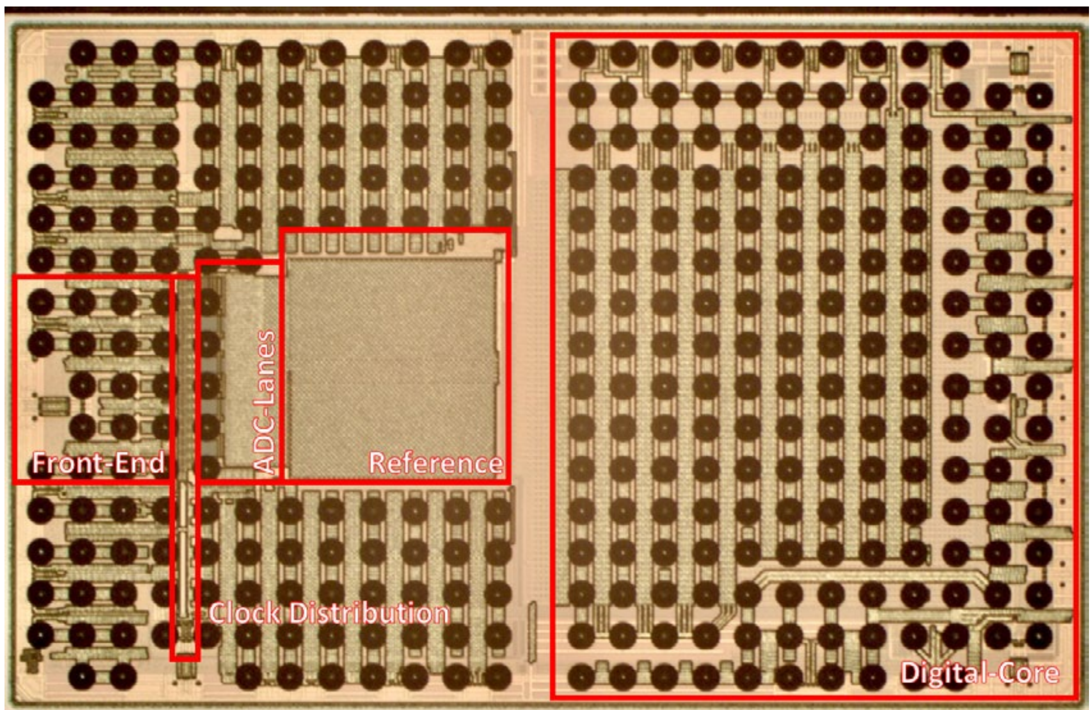

Fig.1: Micrograph of the TI-ADC System.

the SAR algorithm. The design inherently contains an on-chip reference voltage generator, a digital calibration engine covering both SAR-lane and time-interleaved mismatch effects and a JESD204B output interface.

Results

The obtained simulation results are depicted in Figure 2. Given a full scale (1 Vppd) single tone sine wave up to the Nyquist frequency of 4 GHz the ADC system achieves a SFDR of above 73.5 dBc and SNDR above 56 dB across all process corners and the entire input frequency range. The power consumption of the ADC without the digital calibration backend is 1.93 W. Of this, 1.33 W is required for the input buffer topology. With the addition of 1 W required when the digital calibration engine is active, the Schreier FOM yields 148.15 dB for the overall data converter system.

Why EUROPRACTICE?

With the MPW-run program EUROPRACTICE provides the opportunity for universities to access and prototype designs using state-of-the-art technologies of the world-leading foundries such as TSMC 28nm HPC+. EUROPRACTICE provides excellent technical support even shortly before final GDS submission dates.

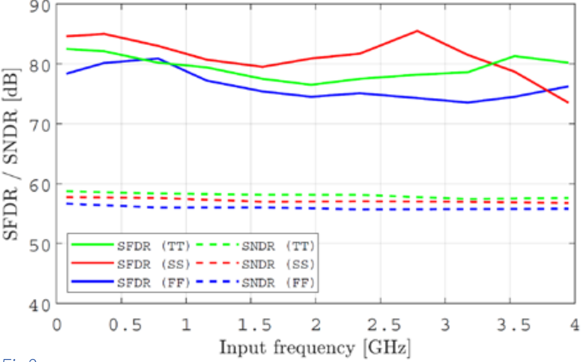

Fig.2:
SNDR and SFDR of the TI-SAR ADC across process corners and input frequency.

Acknowledgements

This work was funded by the German Federal Ministry of Education and Research (BMBF) in the context of the GSADU project (KMU 17/304). Furthermore, we would like to thank our partners from eesy-ic GmbH and LHFT FAU-Erlangen-Nürnberg.

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8-channel chopper based integrated system for biomedical recordings

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Contacts:	P. Kmon, W. Mrzygłód, M. Rosół, P. Wargacki
E-mail:	kmon@agh.edu.pl
Technology:	TSMC 40nm
Die Size:	1.92mm x 1.92mm
Design Tools:	Cadence Virtuoso, Spectre; Siemens Calibre
Application Area:	Biomedical, Sensors

Introduction

The main motivation of the project was to propose an integrated solution that could allow for multichannel recordings of weak biomedical signals. Therefore, we decided to use the modern TSMC 40nm process that allows the implementation of a mixed-mode integrated circuit.

Description

The presented project was realised during one of the courses given on Microelectronics and Technics in Medicine studies - the designer's group of three students was led by the lecturer. The aim of the project was to build a multichannel integrated system dedicated to biomedical signal recordings (i.e. ECG, EMG, neural spikes, LFPs). We proposed the architecture utilising eight chopper-based amplifiers followed by the sample and hold blocks (S/H), the analog multiplexer (MUX), and the ADC. All these blocks require their own clock signal that is locally generated and distributed by the on-chip RC-based oscillator. Input signals are recorded differentially.

Results

We have managed to design, send to fabrication, and start preliminary measurements of the 8-channel integrated circuit dedicated to biomedical recordings. The chip occupies 1.92 x 1.92 mm^2 of silicon area and is composed of the 8 chopper-based amplifiers followed by the 8-bit Analog-to-Digital Converter. All internal blocks are controlled thanks to an on-chip RC-based oscillator providing a 50 MHz clock. The preliminary measurements show that main system parameters are very attractive in terms of biomedical recordings, i.e. the front-end amplifier consumes only 2µA of current, and has 0.96/2.8 µVRMS of input-referred noise (0.5 Hz - 100 Hz)/(100 Hz - 10 kHz) resulting in Noise Efficient Factor equal to only 5.3/1.55. The single recording channel occupies only 0.044 mm^2 of area. The RC oscillator provides 50 MHz on-chip calibrated clock, has Temperature Coefficient equal to only 100 ppm/C, occupies only 0.006 mm^2 of area, and achieves the lowest power consumption per one kHz actually reported (0.92 nW/kHz). The ADC provides 8-bit resolution, is based on SAR architecture of two algorithmic working DAC capacitors, works with 1MS/s rate, and occupies 0.033mm^2.

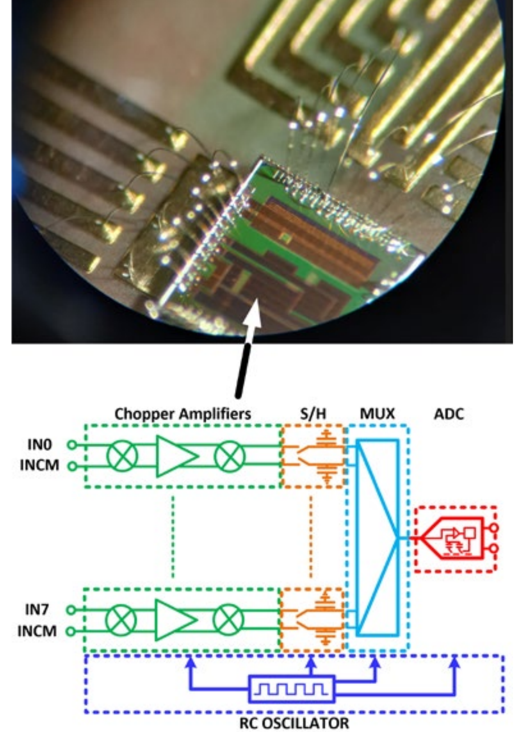

Fig.1: Photo of the PCB mounted chip with schematic idea of the integrated circuit.

Why EUROPRACTICE?

AGH University benefits from the EUROPRACTICE offer for many years, with a lot of successful tapeouts. EUROPRACTICE offers affordable fabrication of our prototypes in MPWs and mini@sics and provides access to a wide variety of design tools. It is an essential partner in our research.

Acknowledgements

The presented work has been supported by the National Science Center, Poland, under Contract No. UMO-2016/23/D/ST7/00488.

References

[1] 8-bit low-power, low-area SAR ADC for biomedical multichannel integrated recording system in CMOS 40nm, Magdalena Rosół, Piotr KMON, MIXDES 2022, 29th international conference on Mixed Design of integrated circuits and systems, 23–24 June 2022, Wrocław, Poland.

[2] A 50 MHz, 46 μW, 0.28% accuracy, 67 ppm/°C relaxation oscillator in 40nm CMOS process for multichannel integrated biomedical recording system, Wojciech Mrzygłód, Piotr KMON, MIXDES 2022, 29th international conference on Mixed Design of integrated circuits and systems, 23–24 June 2022, Wrocław, Poland.

[3] Design of 1.55 NEF, 2μA, chopper based amplifier in 40nm CMOS for biomedical multichannel integrated system, Paweł Wargacki, Piotr KMON, MIXDES 2022, 29th international conference on Mixed Design of integrated circuits and systems, 23–24 June 2022, Wrocław, Poland.

A 10-bit 10 MS/s SAR ADC with Duty-Cycled Multiple Feedback Filter

Eindhoven University of Technology, the Netherlands

Contact: Hanyue Li
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Technology: TSMC 65nm
Die Size: 740µm x 920µm
Design Tools: Cadence Virtuoso
Application Area: IoT

Introduction

Successive-approximation-register (SAR) analog-to-digital converters (ADC) have achieved excellent power efficiency, but their front-end filters may consume even more power than the ADC itself. Therefore, this design aims to develop power saving techniques for filters and improve the power efficiency of the overall system.

Description

This design includes a 10-bit SAR ADC and its frond-end filter. Because the SAR ADC works as a discrete-time data converter, its input signal only needs to be accurate at its sampling moment. Therefore, the filter can be switched off in the ADC conversion phase to save power. To reduce the start-up time when the filter is activated again, a low-power auxiliary amplifier is used in the ADC conversion phase to maintain the filter output roughly. In this design, a classic multiple feedback filter is selected as a proof of concept to validate the feasibility of applying duty-cycled operation to the filter.

Results

The prototype achieves 8.3 ENOB and 59.3 dB SFDR at low input frequencies, and it has 40 dB suppression at the Nyquist input frequency, while consuming 91.1 µW. The filter power has been reduced by 36% with negligible performance degradation, thanks to the proposed duty-cycled operation.

Why EUROPRACTICE?

EUROPRACTICE provides timely and various tape-out options, and we are very satisfied with its service.

Acknowledgements

The work is financed by the Dutch Research Council with project number 16594.

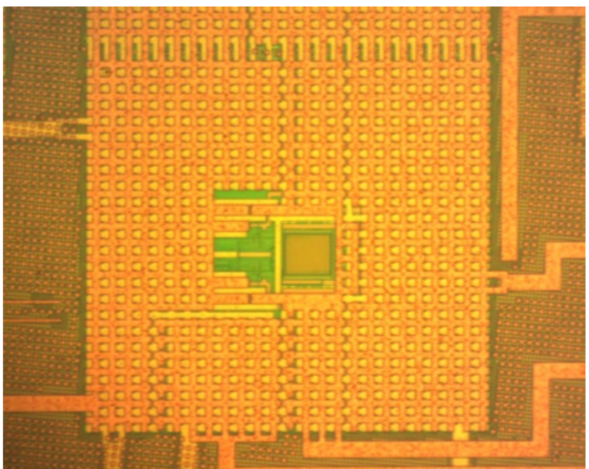

Fig.1: Die photo.

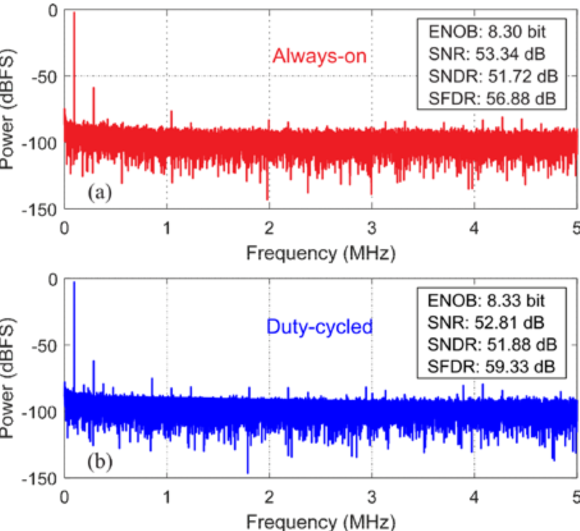

Fig.2: Measured spectrum when the filter is (a) always on or (b) duty cycled.

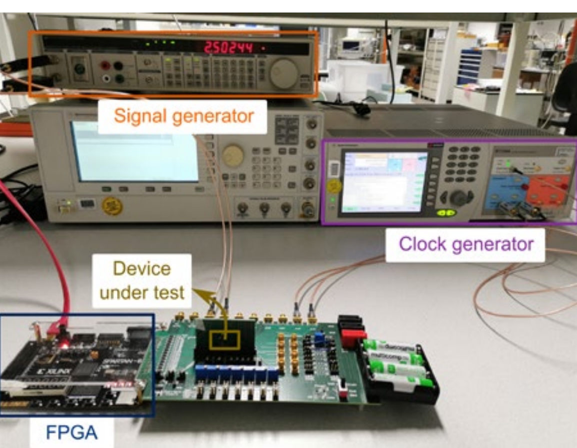

Fig.3: Measurement setup.

A Miniaturized Monitoring System for Implants

INESC-ID, Lisbon, Portugal

Contacts:	Gonçalo Rodrigues, João Silva, Hanna Busse, Diogo Caetano, Taimur Rabuske, Jorge Fernandes
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Technology:	TSMC 65nm
Die Size:	1270µm x 1020µm
Design Tools:	Cadence Virtuoso
Application Area:	Medical / Health

Introduction

Bioelectronic devices are envisioned to be as small as possible (in the mm-sized range). Such miniaturization is currently hampered by the available wireless power transfer techniques, as well as the large volume of conventional hermetic packaging to protect the implants. Alternatively, conformal coatings based on polymers (PDMS) or thin film ceramics are being explored to protect the implant electronics. Such approach has the potential to allow the use of RF energy harvesting and extreme miniaturization. However, the longevity of conformal coatings has not been studied in vivo. In order to address that problem, a fully integrated, compact, mm-sized wireless monitoring system for implants is proposed and designed in TSMC 65nm.

Description

The complete in vivo reliability monitoring system is composed by four major parts: 1. wireless power transfer; 2. Power harvester and rectifier; 3. Resistive humidity sensor and oscillator; 4. Backscattering with amplitude modulation (AM) for data transmission. An overview of the monitoring system is presented in Figure 1.

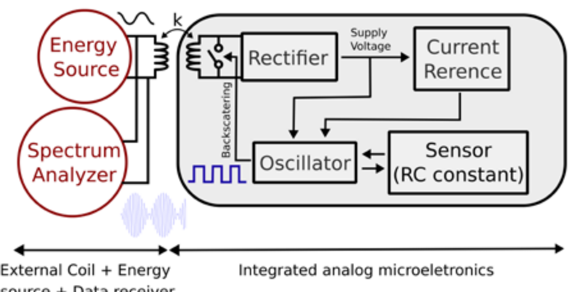

Fig.1: Monitoring System Overview.

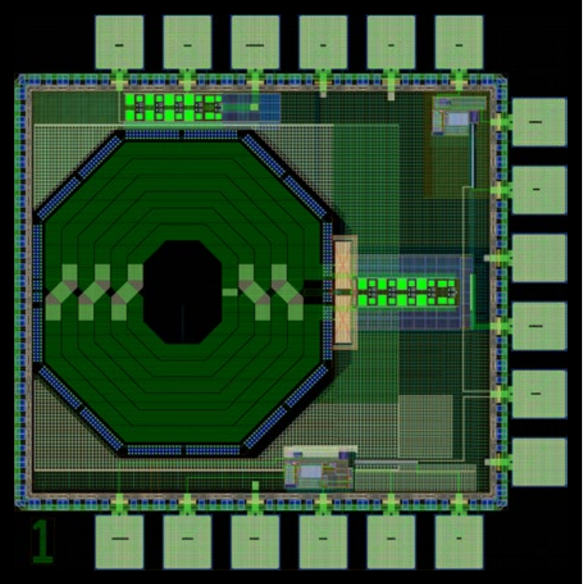

Fig.2: Complete Circuit Layout (LC tank, Rectifier, Oscillator, Current Reference, Oscillator, Sensor Reading Circuitry).

For the wireless power transfer, we opted for an inductive link with a fully integrated coil. This choice strongly limits the amount of power that is supplied to the integrated circuit, however, it simplifies the overall system and allows to have all the components inside the IC.

The received AC wave is converted to a DC supply voltage using a full wave rectifier with dynamic body and gate transistor biasing. The proposed architecture is able to start the rectification process with extremely low input power (- 15dBm) and convert a small amplitude AC signal with 200 mV into a stable 1 V DC.

For the sensor and reading circuitry, an integrated resistivity sensor which is affected by humidity was chosen. This sensor was studied, designed and tested by TU Delf. To read the information of the sensor, a low power, stack ring oscillator is used which changes the operating frequency with an RC time constant.

Finally, in order to transfer the sensor information regarding the hermeticity of the implant, backscattering is used. A switch controlled by the oscillator short circuits the two terminals of the integrated coil in order to change the load and produce an AM modulation on the primary coil. This allows for passive data transfer with the minimum waste of energy.

The circuit layout with the integrated receiving coil, tunning resonant capacitors, rectifier, oscillator, current reference, level shifter, sensor reading circuitry and load modulation is presented in Figure 2. The system is envisioned to be fabricated in the future with no PADs due to the wireless power and data transfer capabilities.

Results

Preliminary results show a stable 15 µW power level available at the output of the rectifier. The complete system was designed to operate under 3 µW so the achieved result gives us some flexibility for coil separation and misalignment.

The ring oscillator frequency is within the expected range, changing from 3 MHz to 8 MHz depending on the sensor resistivity.

Backscattering is yet to be confirmed, due to a slight shift on the LC tank frequency, the inductive link still needs some tunning to reflect the load changes on the secondary side.

On a general note, a fully encapsulated reliability monitoring system was proposed and fabricated. This opens the possibility of monitoring a new generation of implants with conformal coatings.

Why EUROPRACTICE?

We, at INESC-ID, recurrently use the services from EUROPRACTICE due to the excellent communication and concise fabrication process. Starting with the design submission, DRC error solving, wire bonding, packaging and finally shipping. In addition, due to the mini@sic runs, EUROPRACTICE opens the possibility to fabricate prototypes at reasonable academic prices.

Acknowledgements

The authors acknowledge the contributions to all Position-II and Moore4Medical project participants during brainstorm sessions. Special thanks to Kambiz Nanbakhs and Vasiliki Giagka from TU Delft.

This work has been supported by the EU projects funded by the ECSEL JU: POSITION-II under grant number Ecsel-783132-Position-II-IA, Moore4Medical under grant number H2020-ECSEL-2019-IA-876190 and by FCT, Fundação para a Ciência e a Tecnologia (Portugal), under projects UIDB/50021/2020, UNSEEN PTDC/EEI-EEE/31416/2017 and scholarship SFRH/BPD/116007/2016;

An 11 V-tolerant, ultra-compact neurostimulator for high-resolution stimulation in visual prostheses

MICAS Research Group, KU Leuven, Belgium

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E-mails: maxime.feyerick@esat.kuleuven.be, wim.dehaene@esat.kuleuven.be
Technology: TSMC 65nm LP
Die Size: 2mm x 2mm
Design Tools: Cadence suite
Application Area: Medical / Health

Introduction

Over 5 million people worldwide are irreversibly blind as a result of conditions such as glaucoma or age-related macular degeneration. To help these people regain vision, a visual prosthesis, inspired by the success of cochlear implants, is envisioned. To meet this goal, a lot of innovation is still needed from fundamental neurophysiological research all the way to packaging and electrode development. Also the integrated circuits pose a serious research challenge. Many independent channels (>256) are required to achieve sufficient visual resolution for reproduction of a detailed image. This means that each on-chip channel has to be miniaturized. On the other hand, there are two limitations increasing area/channel. First, high-voltage (HV) tolerance (11 V) is necessary to drive the required stimulation currents through the micro-electrodes. Second, the stimulators need to achieve sufficient stimulation charge balance in order to deliver safe stimulation to the tissue: DC error current must be <100 nA. The latter two facts are today impeding high-voltage tolerant stimulators to integrate high channel-counts on-chip.

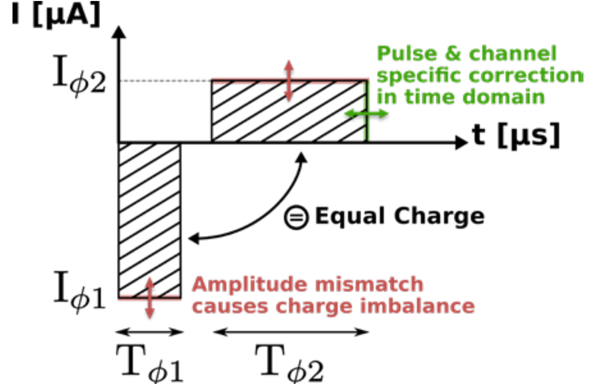

Fig.1: A biphasic current stimulation pulse with the time-domain calibration principle.

Description

Where classical approaches typically add analog hardware at the channel level to achieve charge balance, incurring an area/channel penalty, we opted for a novel, global calibration approach where calibration hardware is shared among all channels. All currents of all channels are measured only once by a global on-chip ADC, after which a channel- and pulse-specific correction in the time-domain is applied (Fig. 1). This approach scales particularly well to larger arrays, where the cost of the global ADC becomes negligible per channel. In combination with an advanced stacking methodology in the electrode driver to achieve 11 V operation in 65nm CMOS, we can use a modern low-voltage CMOS technology to save area in the digital control electronics without sacrificing functionality.

Results

We fabricated a 16-channel prototype to verify the calibration approach and HV circuitry (Fig. 2). The area/channel is only 0.0141 mm², comparable with state-of-the-art low-voltage stimulators. Figure 3 shows various voltage waveforms over pseudo-electrodes which are stimulated by our design. This demonstrates the successful operation of HV electrode driver. After calibration, the stimulation error current is successfully reduced below 59 nA over all channels for all stimulation amplitudes, validating the time-domain calibration approach.

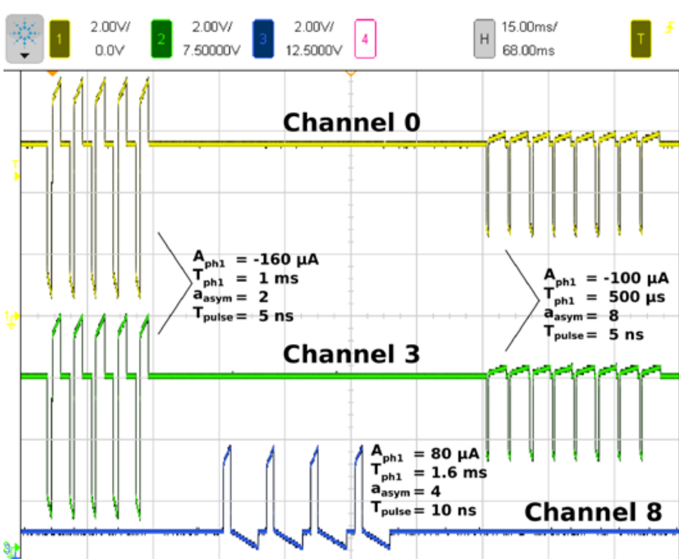

Fig.3: Voltage waveforms over a pseudo-electrode load from various biphasic pulse trains generated by the design.

Why EUROPRACTICE?

The wide portfolio of EUROPRACTICE allows us to choose the right tools and technology for the design. With the mini@sic program, we got an affordable opportunity to test out our research prototype. Now, we are ready to scale-up our design with a next tape-out through EUROPRACTICE.

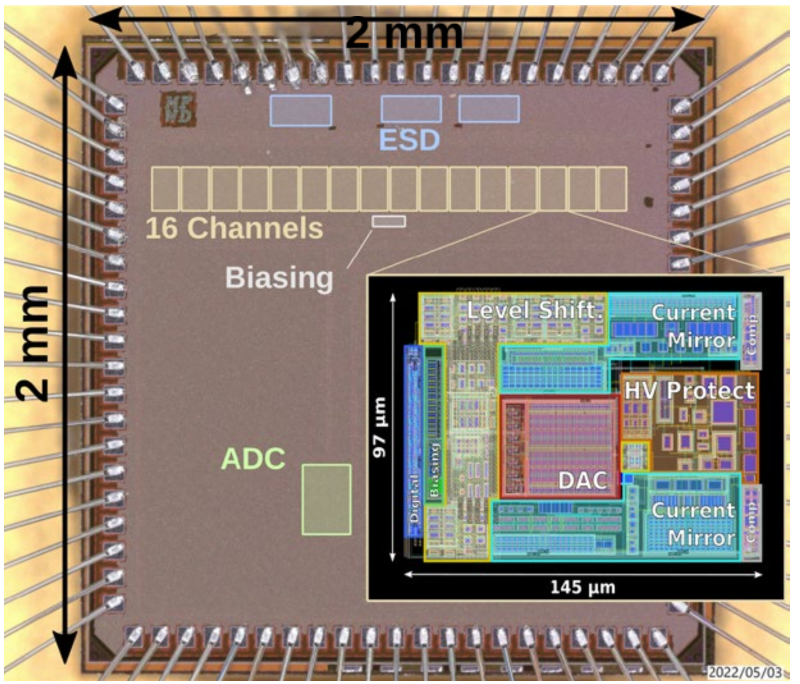

Fig.2: Die picture with annotation of the subblocks.

Acknowledgements

This project has been partially funded by FWO project G0D6520N, "High resolution brain stimulation for visual prostheses".

References

[1] Feyerick, Maxime, and Wim Dehaene. 2022. "An 11 V-Tolerant, High-Density Neurostimulator Using Time-Domain Calibration in 65 Nm CMOS." In 2022 IEEE Biomedical Circuits and Systems Conference (BioCAS), 429–33. https://doi.org/10.1109/BioCAS54905.2022.9948626

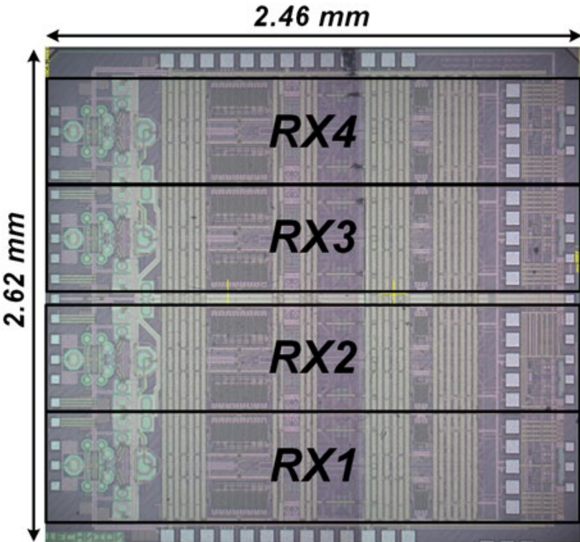

Fig.1: Micrograph of the manufactured chip.

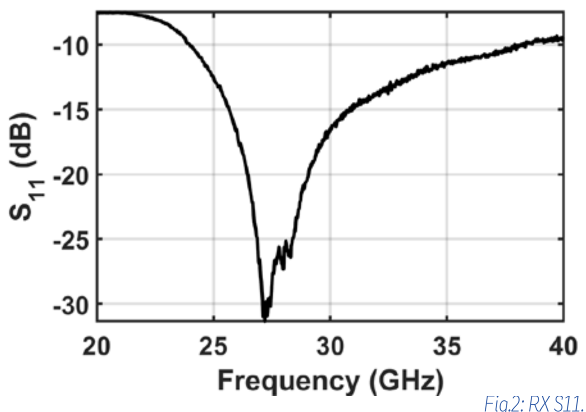

Fig.2: RX S11.

A 28 GHz Blocker-Tolerant Phased-Array Receiver Array With Digital Beamforming

High frequency Integrated Circuit (HFIC) Lab, Faculty of Electrical Engineering, Technion, Haifa, Israel

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E-mails:	zoerez@campus.technion.ac.il, nimrodg123@gmail.com, emcohen@ee.technion.ac.il
Technology:	TSMC 65nm LP
Die Size:	2.46mm x 2.62mm
Design Tools:	Cadence Virtuoso
Application Area:	Datacom / Telecom

Introduction

As the RF spectrum becomes increasingly crowded, higher frequency bands are becoming available such as mmW for 5G communication. At the same time next generation of mobile wireless is expected to have digital beam-forming arrays with high spatial flexibility for massive MIMO channel capacity enhancement. As spatial filtering is performed at the baseband single receiver front-end requirement of linearity is increased. Thus, to most effectively utilise the 5G spectrum, receivers must be capable of resistance tolerance to interferer at other frequencies and instantly-tune across frequencies.

This device presented here addresses the challenge of implementing a fully integrated digital phased-array receiver capable of withstanding powerful out-of-band (OOB) blockers, without sacrificing performance or power, omitting the need for an external filter for TX-RX isolation.

Description

This device comprises four 28 GHz OOB blocker-tolerant receiver (RX) chains for a 4 antenna elements phased array using N-path filters at RF frequencies with TIA without degrading system NF. The RXs are fed by a single PLL, whose power is split between all RXs by on-chip Wilkinson power splitters.

Results

Each receiver achieves the following KPIs:

1. <-10 dB S11 between 24-38 GHz
2. NF<4 dB at 24-28 GHz
3. RX gain of 37 dB with 200 MHz RF bandwidth and 80 dB/ dec baseband filtering
4. -3.5 dBm B1dB at >500 MHz offset
5. In-band (IB) IIP3 of -12 dBm and OOB IIP3 of 10 dBm
6. IB IIP2 of 20 dBm and OOB IIP2 of 65 dBm

To our knowledge, this is the first 28 GHz RX that achieves simultaneous low NF and high B1dB. By using our device, phased array transceivers can be manufactured without the need for an external filters and can meet high linearity requirement of a digital mmW array.

Why EUROPRACTICE?

We selected EUROPRACTICE to manufacture this chip and other previous ones because their services are suitable for our academic research needs. They have provided us with technical support throughout the process, thanks to their extensive experience with TSMC's processes. Additionally, EUROPRACTICE offers affordable prices, which makes it financially feasible for our research group to explore different designs. They also have a high level of availability and consistently deliver on time.

Next generation neuromorphic BrainScaleS-2 SoC

Electronic Vision(s) Group, Kirchhoff-Institute for Physics, Heidelberg University, Germany

Contact:	Dr. Johannes Schemmel
E-mail:	schemmel@kip.uni-heidelberg.de
Technology:	TSMC 65nm
Die Size:	8mm x4mm
Design Tools:	Cadence Virtuoso, Innovus; Siemens Calibre; Synopsys Synthesis
Application Area:	AI

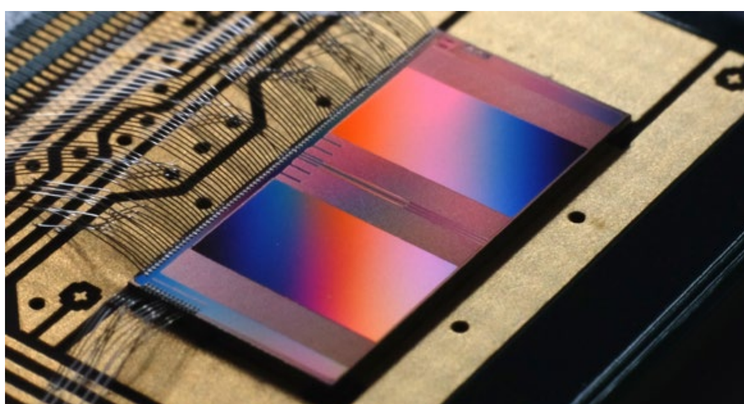

Fig.1: Photograph of the fabricated ASIC.

Introduction

BrainScaleS-2 is a family of mixed-signal neuromorphic ASICs developed at Heidelberg University. This tape-out marked the latest revision and builds on top of the success of its predecessors. It allows the accelerated emulation of spiking neural networks (SNNs) for both the exploration of energy-efficient, brain-inspired machine intelligence and the emulation of complex, even multi-compartmental neuron and network models. The current revision features a number of incremental improvements as well as fundamentally new subsystems, including a complete redesign of the neuron circuit, which now features a flexibly configurable and accurate emulation of the complete adaptive exponential leaky integrate-and-fire model.

Description

A BrainScaleS-2 ASIC features an analog neuromorphic core consisting of 512 neuron compartments and a total of 512 × 256 synapses. These circuits emulate neuronal and synaptic dynamics with a 1000-fold acceleration in comparison to biological real-time. BrainScaleS-2, furthermore, features complex synapse dynamics on both short and long timescales through the implementation of short-term as well as spike-timing-dependent plasticity. Importantly, the analog core is augmented by a rich digital periphery: An on-chip event router allows the configuration of almost arbitrary network topologies, the recording of internal spikes, as well as the injection of external events. Communication between the ASIC and its host periphery is enabled through eight links capable of an aggregated bandwidth of up to 32 Gbit/s. The analog core is, however, most importantly accompanied by a pair of embedded microprocessors implementing the Power-PC instruction architecture with a custom 128bit-wide SIMD vector extension for an efficient interfacing with the parallel analog core. They are, for that purpose, combined with a massively parallel 8bit ADC array with a total of 1024 channels. The combination of the efficient and fast emulation of time-continuous network dynamics in analog circuits with the flexibility of interacting with those dynamics from the embedded processors allows for a wide spectrum of applications: They range from on-chip calibration routines to the exploration of synaptic plasticity algorithms as well as the simulation of closed-loop environments on the ASIC itself.

Results

The redesigned neuron circuits are one of the most prominent additions introduced by the latest revision. Their dynamics accurately follow the adaptive exponential leaky integrate-and-fire equations and can be tuned to a wide range of parameters, facilitating the emulation of a plethora of target dynamics similar to the ones observed in electrophysiological recordings. This includes, i.a., adapting, accelerating, and bursting behavior as well as the interplay of neurons structured in multiple compartments.

Why EUROPRACTICE?

Heidelberg University has worked with EUROPRACTICE on TSMC and other IC fabrication on a multitude of successful tapeouts since 1994. EUROPRACTICE has been a reliable partner for all aspects of multi-project and full mask set prototypes. The affordable access to multi-project wafer and mini@sic fabrication has been an enabling factor for our research in neuromorphic hardware.

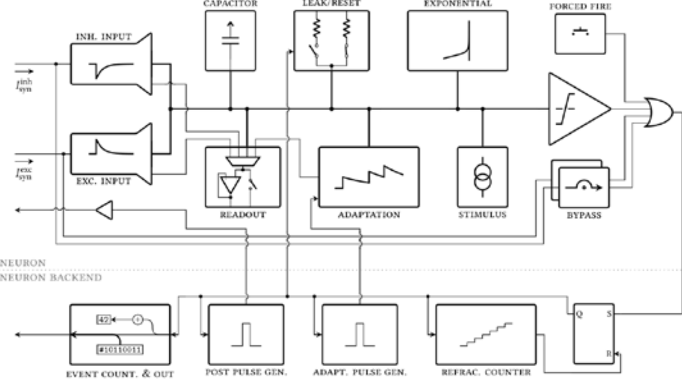

Fig.2: Schematic overview of the silicon neuron design including the analog circuits emulating the time-continuous dynamics and the full-custom digital backend.

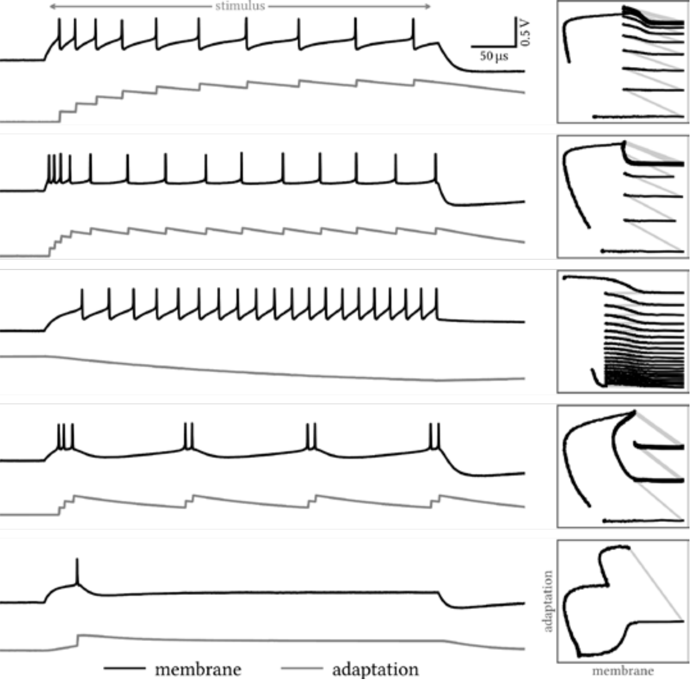

Fig.3: Exemplary firing patterns demonstrated in recordings of the analog silicon neuron's membrane and adaptation state voltages.

Acknowledgements

The research has received funding from the European Union's Horizon 2020 Framework Programme for Research and Innovation under the Specific Grant Agreement Nos. 720270, 785907 and 945539 (Human Brain Project, HBP), the Helmholtz Association Initiative and Networking Fund [Advanced Computing Architectures (ACA)] under Project SO-092.

5-GHz CMOS LNA for interfacing Spin-Hall Nano-Oscillators for neuromorphic computing

Instituto de Microelectrónica de Sevilla (IMSE-CNM), CSIC and Universidad de Sevilla, Spain

Contact:	Rafaela Fiorelli
E-mail:	fiorelli@imse-cnm.csic.es

Technology:	TSMC 0.18µm
Die Size:	1650µm x1100µm
Application Area:	High Performance Computing (HPC)

Introduction

Hall-effect nano-oscillators are promising devices that go beyond CMOS and can be used to emulate the functioning of neurons in computational neuromorphic systems. As they oscillate in the 4-20 GHz range, they could be used to build highly accelerated neural hardware platforms. On the other hand, due to their extremely low signal level and high output impedance, as well as their operating frequency in the microwave range, discerning whether the SHNO is oscillating or not is a major challenge when their state-readout circuitry is implemented using CMOS technologies. This chip features a 180nm CMOS LNA working in the 5-GHZ frequency range that implements the first block of a Front-End that realises this implementation.

Description

Considering the novel idea of using neuromorphic computing systems with neural Spin-Hall Nano Oscillators (SHNO), we present a chip that implements a narrow-band, single-to-differential Low Noise Amplifier (LNA) balun, working in the 4 GHz-5 GHz band. Due to the low noise levels of the SHNO (below -160 dBm/Hz), its low SNR (~15dB), which results in signals below 100uV at output, and its high output resistance (in the order of 300 Ohms or more, far away from the typical 50 Ohms), its design is extremely complex when working in frequencies near the microwaves and using a 180-nm technology node. Since the SHNO is a single-ended output device, and the LNA will be placed in a front-end with a differential architecture, we chose the narrowband single-ended to differential balun-LNA architecture of [1]. The microphotograph of the LNA is shown in Figure 1, occupying an area of 660µmx740µm.

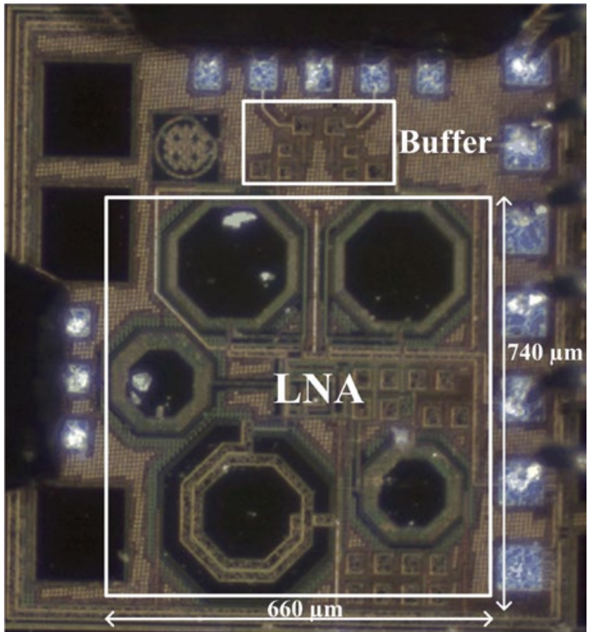

Fig.1: Microphotograph of the NB balun LNA.

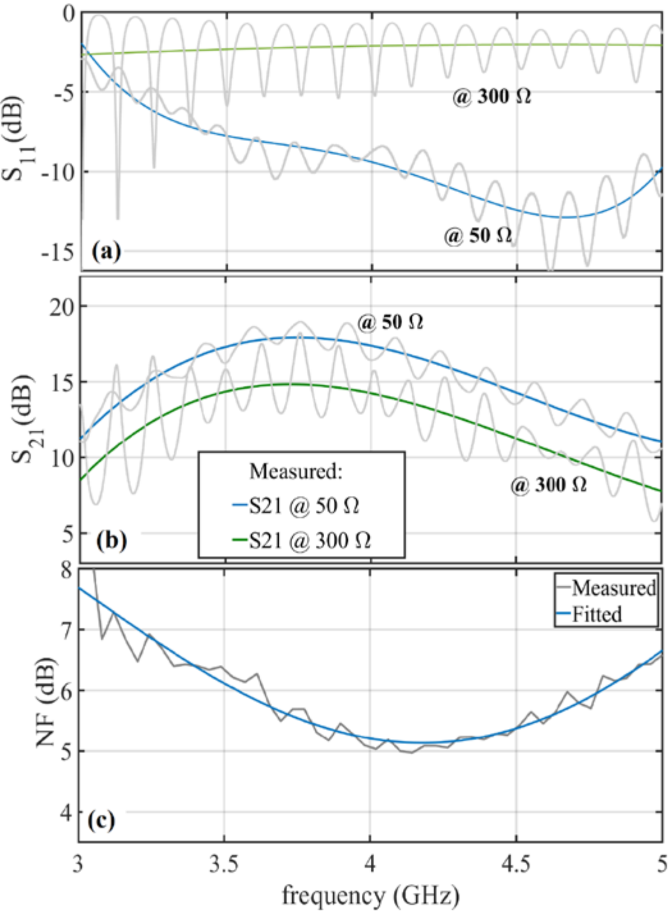

Fig.2: Characterization of the fabricated NB balun LNA: measured (grey) and fitted (blue, green) for: (a) S11, (b) S21, (c) NF.

Results

The designed single-to-differential balun LNA drains 5.4mA at 1.8V. Its characteristics of S11, S21 and Noise Figure (NF), measured using picoprobes, are plotted in Figure 2. When measured at 50 Ohms, S11,min= -13 dB @4.7GHz, S21,max =17.9 @3.8GHz and NFmin=4.9 @4.1GHz.

Transforming these measurements to the expected 300-Ohms SHNO output resistance, its gain is 14.8 dB@3.8GHz. As expected, the imposition of working with such high output resistance drastically worsens the LNA's input matching, gain and noise figure, as well as its power consumption. In spite of this, when working at the frequency of minimum noise figure, the gain achieves values above 14 dB.

Why EUROPRACTICE?

The Institute of Microelectronics of Seville has been using EUROPRACTICE services for many years. EUROPRACTICE program offers designers and researchers the opportunity to prototype their designs at an affordable price. As well, EUROPRACTICE staff are very responsive and helpful, provide excellent technical support through the different stages of the tape-out.

Acknowledgements

This research was funded by the Horizon 2020 Research and Innovation Program No. 899559 SpinAge.

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MalariaChip

University of Minho, Portugal

Contacts:	Graça Minas, Susana Catarino
E-mails:	gminas@dei.uminho.pt, scatarino@dei.uminho.pt
Technology:	UMC L180 MM/RF
Die Size:	1525µm x 1525µm
Application Area:	Medical / Health

Introduction

It is an academic project for the medical/health area. This chip intends to be implemented in a portable and autonomous device for malaria diagnosis through optical spectrophotometry, complemented by acoustic sensors for blood flow assessment

Description

The final end-use of the chip is the integration of the academic prototype into a miniaturized device for malaria diagnosis.

The chip comprises 16 photodetectors (4 x 4 array), current to frequency converters (one per photodiode), acoustic sensor (VCO, operational amplifier and a logic circuit to compare two signals) and RF circuits.

The chip detects the optical absorption of blood samples in the visible spectrum range (400nm to 800nm) measuring the intensity of the light that passes through the blood samples (the samples are in a cuvette positioned on top of the photodiodes) in 16 wavelengths of that spectrum range. As the malaria disease progress, it forms a crystal inside the Red Blood Cells (RBC), the Hemozoin (Hz), which has a specific spectral fingerprint. The healthy RBCs do not have Hz and their optical spectra have a different shape than the RBCs infected with Hz. These differences are used to optically determine the presence and the intensity of the Hz and thus related to the disease.

Results

Using the designed photodiodes, we were able to detect differences between the optical spectrophotometry signals of healthy blood and blood infected with malaria parasites (Plasmodium falciparum), up to 12 parasites/uL of red blood cells.

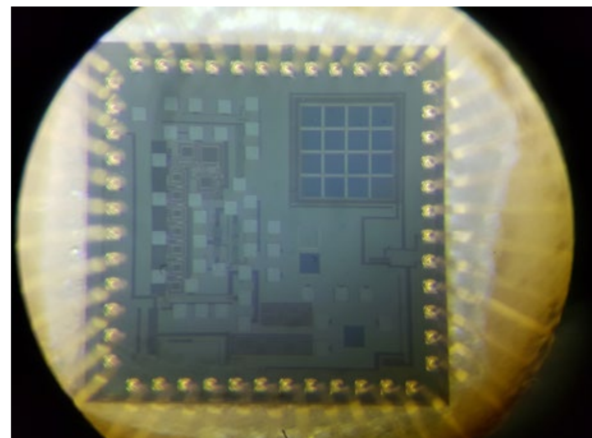

Fig.1: Microscope photograph of the 0.18µm fabricated die.

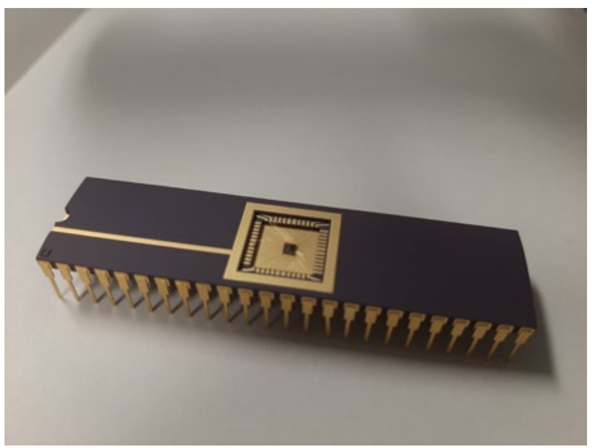

Fig.2: Photograph of the die after wirebonding and encapsulation.

Why EUROPRACTICE?

As we are a EUROPRACTICE member, EUROPRACTICE has accompanied us for many years and helped us in the fabrication of several microsystems. Always ensured professional communication and quality CMOS chips.

Acknowledgements

This work was supported by Project PTDC/EEI-EEE/28178/2017, NORTE-01-0145-FEDER-028178 funded by NORTE 2020 Portugal Regional Operational Program under PORTUGAL 2020 Partnership Agreement through the European Regional Development Fund and the Fundação para a Ciência e Tecnologia (FCT), IP.

References

We have submitted a manuscript to the IEEE Journal: Transactions on Biomedical Engineering and it is at that moment under revision.

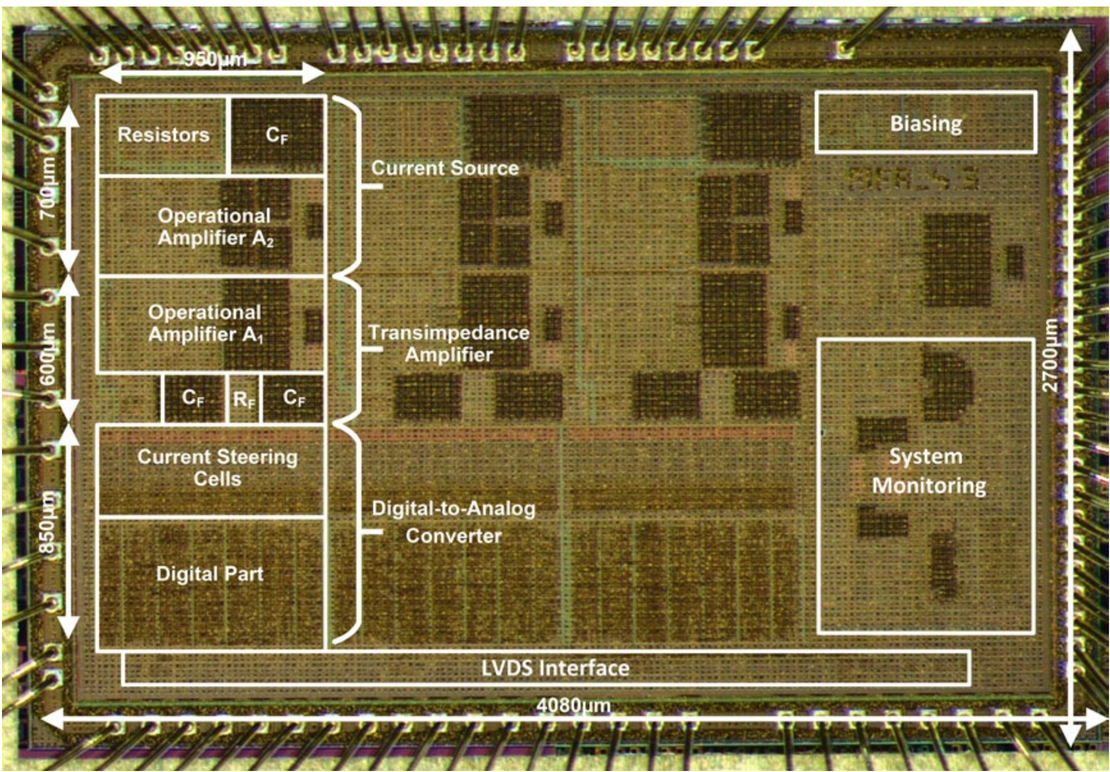

Fig.1: Microphotograph of the fabricated chip.

High Precision Magnetometer Front-End ASIC

Institute of Electronics, Graz University of Technology and Space Research Institute, Austrian Academy of Sciences, Austria

Contacts:	Maximilian Scherzer, Mario Auer, Aris Valavanoglou, Werner Magnes
E-mail:	maximilian.scherzer@tugraz.at
Technology:	X-FAB XH018
Die Size:	4080µm x 2700µm
Design Tools:	Cadence
Application Area:	(Aero)Space

Introduction

Fluxgate sensors are used to measure magnetic fields with a very high resolution. In the presented design a spaceborne application is targeted. To increase the linearity and measurement range of the system the ambient magnetic field is compensated within the sensor using an additional feedback coil hereby creating a closed loop system. The performance of a magnetometer instrument is ultimately limited by the current source of the feedback path. This feedback path consists of a high resolution digital-to-analog converter, a subsequent signal conditioning block and a current source to drive the feedback coil. The D/A conversion is realized with a current-steering DAC. In order to enable measurements of the Earth's magnetic field, currents of up to 18mA must be provided by the current source. This current is then used to compensate the ambient magnetic field and therefore the linearity of the measurement is limited by the quality of the current source. The design is constrained by the limited supply voltage and the voltage drop across the load (almost 1.5 V).

Description

The designed chip consists of a digitally controlled fully differential low noise current source. It was designed to be used in the feedback path of a fluxgate magnetometer, however, the concept is applicable wherever a low noise and precise current is required. The current source is driven by a transimpedance amplifier that buffers the output of a current-steering digital-to-analog converter. A detailed analysis of the design is shown in [1].

Results

A total of 5 samples have been characterized with an experimental setup that includes an Audio Precision APx555 analyser. The maximum signal-to-noise ratio for a bandwidth of 512 Hz is 98.3 dB for a sinusoidal input with 37 Hz. The performance of the current source is limited by the total harmonic distortion of 80 dB. The measured average noise floor for the frequency band of interest is lower than 5.5 nA/√Hz resulting in a noise level of 20 pT/√Hz for a given fluxgate sensor. However, the resulting magnetic noise level is very much depended on the feedback coil constant of the used fluxgate sensor. Moreover, the output impedance of the current source was evaluated as well, resulting in an average value of 205 kΩ. The realized front-end enables highly accurate magnetic field measurements of up to 65000 nT and is only limited by the measured total harmonic distortion of 80 dB. In addition, the miniaturization of the electronics is crucial, since a dense and lightweight circuitry is a key enabler for space missions that rely on cube satellites. Within this

funded project the presented work is a key element of the FORESAIL-2 spacecraft, a future CubeSat mission operated along the geostationary transfer orbit, hereby serving as a technology demonstration.

Why EUROPRACTICE?

The Graz University of Technology - Institute of Electronics, has worked with EUROPRACTICE for several years. EUROPRACTICE Services provide access to design support and process design kits. Besides, EUROPRACTICE offers excellent technical support for DRC verification and GDS submission. Finally, EUROPRACTICE provides access to different technologies at affordable price.

Acknowledgements

This research work of the Space Research Institute of the Austrian Academy of Sciences and the Institute of Electronics of the Graz, University of Technology was co-funded by the Austrian Space Applications Program (project no. 878878), which is managed by the Austrian Research Promotion Agency.

References

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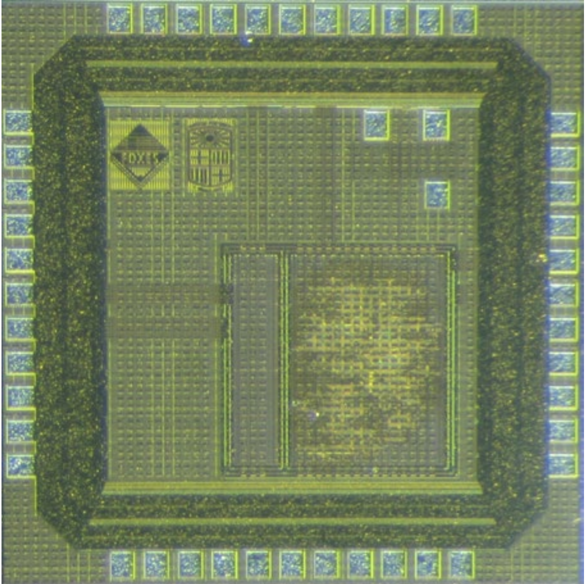

Fig.1: Picture of the FOXES_DIG_V1 chip.

FOXES_DIG_V1: ultra-low power digital controller of an IoT sensor node supplied by a power source made of environmentally friendly materials

University of Barcelona, Spain

Contacts: Oscar Alonso, Juan L. Soler, J. Daniel Prades

E-mails: oalonso@ub.edu, j.soler@ub.edu, dprades@ub.edu

Technology: XFAB XH018

Die Size: 1.5mm x 1.5mm

Design Tools: Cadence

Application Area: IoT

Introduction

The research aims at demonstrating the possibility of powering a fully functional autonomous sensor node with energy harvesting components completely made of environmentally friendly material. This energy harvesting unit (Power Cube) integrates the harvester (4 lead free perovskite solar cells), a primary energy storage (a lead free perovskite thin film supercapacitor) and the power management circuits to supply a regulated output to the load (the IoT Bundle) and/or to a secondary energy storage (a highly porous carbon supercapacitor). The design involved in this application relates to the IoT Bundle, which is the functional

component and demonstrates that powering a smart system using only green harvesting materials is possible. This IoT Bundle integrates an Ambiental sensor, the corresponding measurement electronics, the system control logic and the wireless communications. It must have a power consumption below 50µW in order for the Power Cube to be able to sustain the circuit power.

The ASIC described here (FOXES_DIG_V1) is the second from a series of three chips:

1. FOXES_ANA_V1: Analog circuits to drive and measure the sensor.
2. FOXES_DIG_V1: Digital blocks to control and take measurements from the FOXES_ANA_V1 periodically, process the already digitalized measures, save the data into an external non-volatile memory and send all the results through a wireless module (LoRa).
3. FOXES_V2: mixed ASIC combining the two previous chip to optimize power and performance.

Description

The 44 pin device presents two main blocks, the first includes the control logic and the processing modules for the FOXES_ANA_V1 chip and, the second, contains the control logic to save the sensor measurements in the external memory and for them to be sent via a LoRa wireless module. To achieve those functions, the system incorporates a control unit for each circuit of the analog chip (Current DAC for the LED driver, current source to bias the resistive layer of the sensor, a voltage measurement unit and a resistive dependence oscillator), a memory controller that uses an SPI to communicate with the external non-volatile RAM, a LoRa controller that also has an SPI to talk with the radio so it can send the data, a system controller to organize the timing of each sub-block procedure, a power management unit and a timer to generate a tick periodically indicating a new measurement has to take place.

To reduce the consumption of the chip, we have two power domains in the system, one addressing the IO power to use 1.8V logic level signals and a 1.2V core, it also presents clock gating technique and power optimized finite state machines. The ASIC is designed to withstand a clock frequency of 20MHz.

Results

The chip was received in October and it is still under test.

Why EUROPRACTICE?

EUROPRACTICE grants access to several foundries and to design tools by fixing prices that are affordable for researchers. In our particular case, EUROPRACTICE allows us to access mini@sic runs, where we can integrate and test different designs to choose the best ones that fit our research activities

Acknowledgements

This work was supported by the European Union's Horizon 2020 Research and Innovation Programme, under grant agreement Nr. 951774.

Two monolithic active pixel sensors in the XT018 technology

Czech Technical University in Prague, Czech Republic

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Technology:	X-FAB XT018
Design Tools:	Cadence

Chip 1: a novel monolithic pixel detector for X-ray imaging X-CHIP-04

Die Size:	3960µm × 4760µm
Application Area:	High Energy Physics (HEP)

Introduction

X-CHIP-04 is monolithic active pixel sensor developed for soft X-ray imaging and advanced dosimetry designed in 180nm high voltage (HV) silicon on insulator (SOI) CMOS technology (Fig. 1). Novel feature of this sensor is capability to operate in two modes: hit counting mode (X-ray imaging) and ADC mode (advanced dosimetry). The hit counting mode is primarily designed for radiation imaging and the ADC mode is intended for measurement of energy deposited in each pixel.

Description

X-CHIP-04 is a monolithic active pixel sensor with a 64x64 pixel matrix. Dimensions of pixels are 60µm x 60µm. The analog signals from pixels are sampled by 10-bit SAR ADCs in ADC mode or stored in 16-bit counter in Hit Counting mode. Readout digital part offers 400 MHz LVDS or 50 MHz SPI interface. The input dynamic range is from 1ke- to 10ke-. Threshold for TID effect is 2 kGy @ 15 Gy/min.

Results

To demonstrate the spectral performance measurements with radioactive sources (55Fe and 238Pu) and X-Ray fluorescence were performed. The spectral lines can be seen in Figure 2. Figure 3 demonstrates X-CHIP-04 X-ray imaging capabilities.

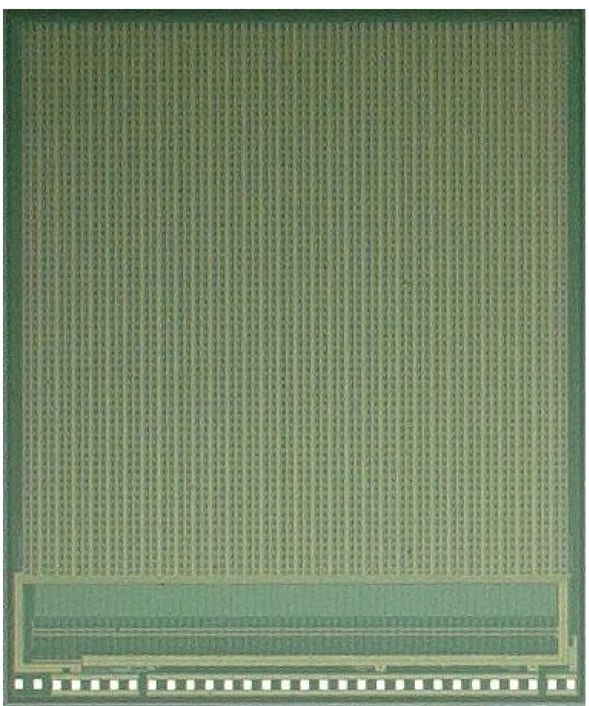

Fig.1: X-CHIP-04 ASIC.

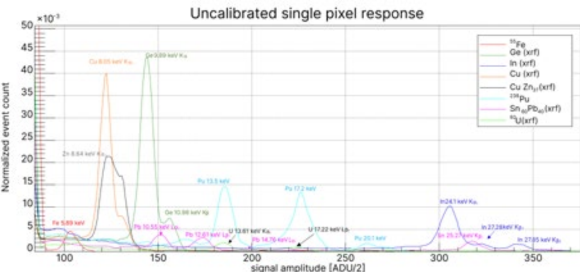

Fig.2: Single-pixel response in ADC mode to soft X-rays.

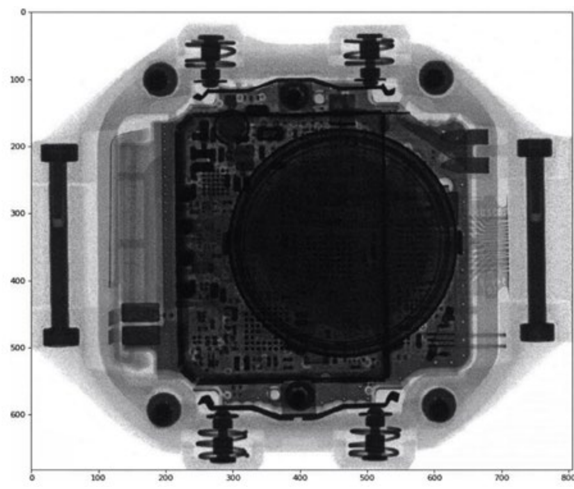

Fig.3: An X-ray image of a wristwatch.

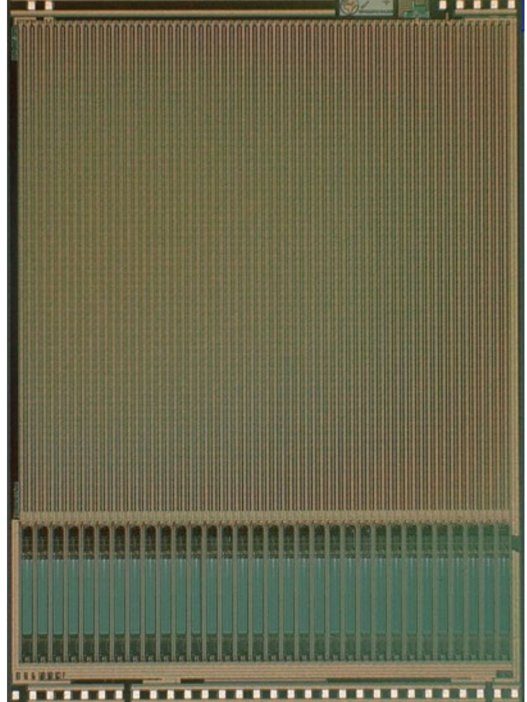

Fig.1: SpacePix3 ASIC.

Chip 2: SoI MAPS Detector for Space Radiation Monitoring SpacePix3

Die Size:	3960µm × 5600µm
Application Area:	(Aero)Space

Introduction

Space radiation is an obstacle for manned and robotic missions and space infrastructure. Radiation in space has several components with large variation of flux and deposited energy. Most important components (with regard to radiation effects) are charged particles: electrons, protons, and heavy ions. Pixel detectors are optimal tools for detection of such radiation and are able to measure flux and linear energy transfer (LET).

Description

SpacePix3 is a monolithic active pixel sensor with a 64x64 pixel matrix (Fig. 1). Sensitive area is 3.84mm x 3.84mm with pixel size of 60µm x 60µm . The analog signals from pixels are sampled by 10-bit SAR ADCs. The total current consumption is 43 mA. Readout digital part offers 400 MHz LVDS or 50 MHz SPI interface. The input dynamic range is from 2ke- to 80ke-.

Results

SpacePix3 is a part of the Czech nanosatellite VZLUSAT-2 mission as a component of the SpacePix Radiation Monitor. Received VZLUSAT-2 data can be seen in Figure 2. Even though the dynamic range of the SpacePix3 amplifier is optimized for space radiation, it can distinguish X-ray peaks from Pu-238 which can be seen in Figure 3.

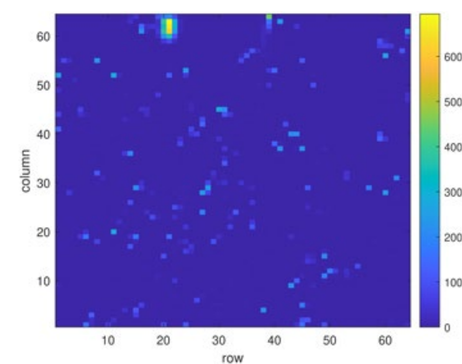

Fig.2: Pu-238 spectrum measured by SpacePix3.

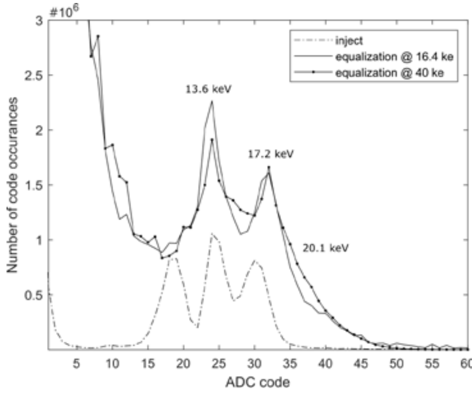

Fig.3: South Atlantic Anomaly measured in orbit at Czech nanosatellite VZLUSAT-2 mission.

The technology promises to design circuits with high radiation tolerant level. Together with the radiation hardening design concept, SpacePix presents a novel detector capable of operating in the space environment.

Why EUROPRACTICE?

Our research group has been cooperating with EUROPRACTICE for several years already. A EUROPRACTICE consortium partner imec provides excellent technical support which is crucial for successful submission of designs. imec is also very helpful with all the administrative issues. The staff is very responsive and highly qualified. Thanks to EUROPRACTICE we have access to different technologies at an affordable price.

Acknowledgements

The work was supported from European Regional Development Fund-Project Center of Advanced Applied Science No. CZ.02.1.01/0.0/0.0/16-019/0000778.

Photonic integrated optical time domain reflectometer

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E-mail: monbasli@ku.edu.tr

Technology: iSiPP50G
Die Size: 25.4mm x 25.4mm per die
Design Tools: Lumerical
Application Area: Open-Source Hardware

Introduction

Optical time domain reflectometry (OTDR) is a distributed sensing method. It is used for structural deformation monitoring of bridges, tunnels, and buildings, temperature monitoring, earthquake detection, vibration sensing, acoustic noise and signal detection, biosensing and homeland security applications (i.e., intrusion detection, monitoring of pedestrians, vehicles, manual digging or excavation near mines or pipelines). The field deployment of OTDR systems consists of fiber optical systems which are vulnerable to simultaneous thermal and strain-induced instabilities in the Raman and Rayleigh scattering signals. State-of-the-art OTDR receivers and transmitters are bulky optical boxes that increase the system cost significantly. As a result, to minimize the confounding thermal and strain effects and to reduce cost of the OTDR system, miniaturization of these parts into a single chip could be a useful solution. By stabilizing the temperature of the photonic integrated OTDR transceiver chip, pure strain effects can be read out. In addition, the unit cost could also be reduced so that field deployment, maintenance and future data mining and machine learning applications could be used.

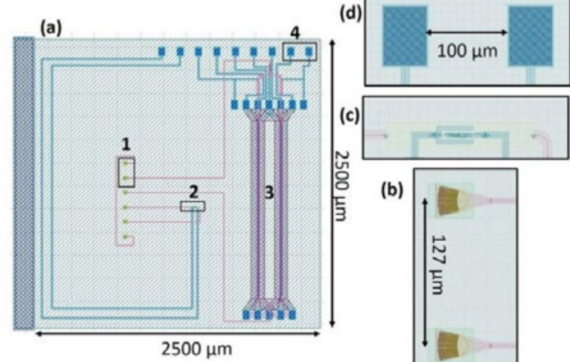


Fig.1: Optical time domain reflectometer (OTDR) chip layout used for our iSiPP50G tapeout with imec.

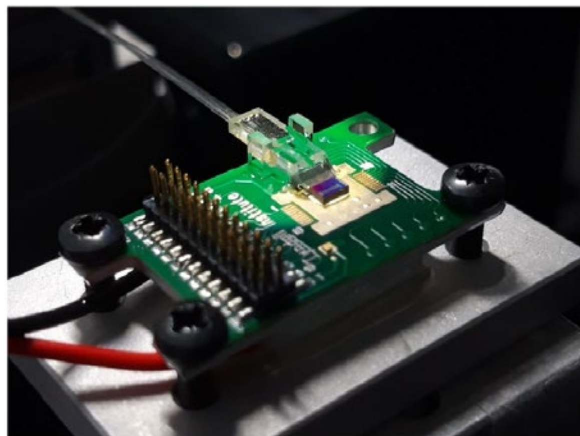
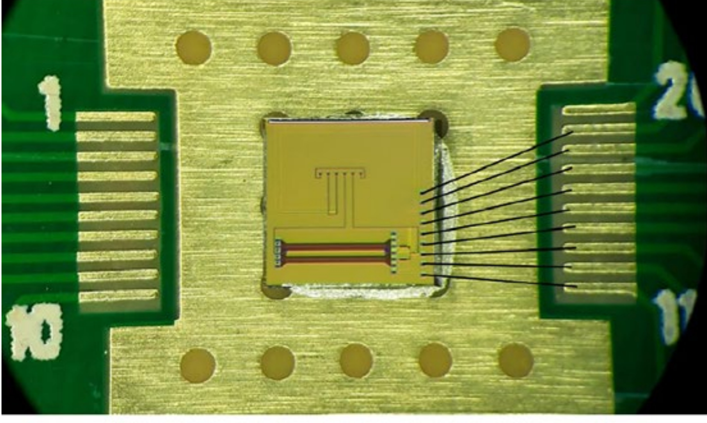


Fig.3: Photo of the packaged optical chip.

Photonic integration could help use the miniaturization and the potential cost advantages of integrated components. By using multi-project wafer fabrication runs, we believe OTDR-based distributed sensing applications could be improved and their costs could be reduced.

Description

OTDR chips work on the principle that if there is a strain or temperature-driven anomaly on an optical fiber, the local change in the fiber's refractive index causes reflection on a laser pulse sent on it. The time difference between the initialization of the pulse and the detection of the reflected part helps



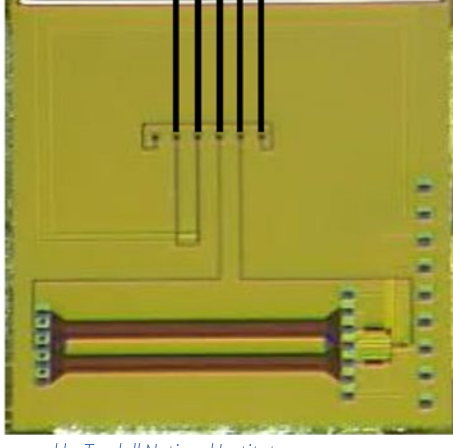


Fig.2: Optical microscope image of electrical and optical connections on one of our chips, as prepared by Tyndall National Institute.

determine the location of index change on the fiber. Depending on the position as well as the refractive index change amount and the Raman peak intensity change, one can determine if a disturbance is a temperature change, strain change or both and their locations as well.

In our design, we combine the transmitter and the receiver side of an OTDR module into a single photonic integrated circuit and use silicon photonics to achieve low-cost integration. The transmitter side includes a fiber Bragg grating, a Mach-Zehnder modulator (MZM) as a software-controlled pulse forming unit, and another fiber Bragg grating to couple light out to the km-long fiber for distributed sensing. The MZM resonances can be tuned to match the exact laser wavelength by using the MZM's integrated microheaters. Laser is externally connected to the chip for modular applications.

On the receiver side, the circuit contains a fiber Bragg grating, integrated Ge waveguide photodetector and another fiber Bragg grating. These items ensure independent testing of the components. For this round of run, balanced detection was not chosen to ensure that the most fundamental functionalities can be achieved within the die space.

Results

The final chip layout is shown in Figure 1. Tyndall National Institute's packaging solution for our die is shown in Figures 2 and 3. The initial testing results are shown in Figure 4, which contains the transmission spectra. Although the modulators have not yet been tested in our lab, we previously analysed that the circuit (Turkish Journal of Electrical Engineering & Computer Sciences 30 (3), 579-591 (2022)) and that it has sufficient power margin to operate over at least a 40 km-long fiber. In addition, we can analyse strain and temperature independently by doing simultaneous spectral and temporal pulse analysis (Front. Phys. 7:155 (2019); Sensors 13, 1836 (2013); Sensors 20(22), 6594 (2020)). We plan to start testing the chips in our lab as soon as we receive the packaged chips from the customs.

Why EUROPRACTICE?

EUROPRACTICE provides the tools and the community for designing a number of different chip technologies and refining them. In particular, it helps us access imec's multi-project wafer runs (MPW), especially the actives such as iSiPP50G, which contains detectors and modulators.

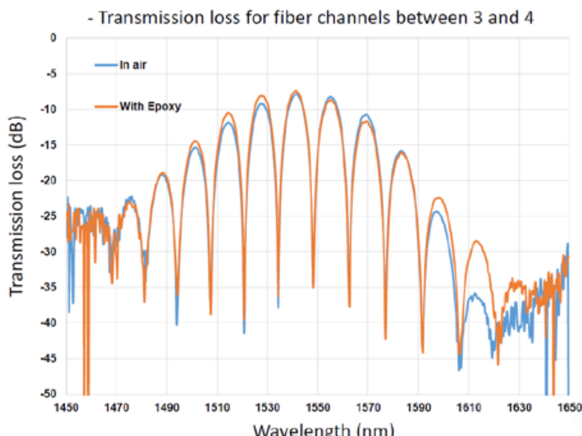


Fig.4: Measured transmission spectra of the chip (spectral measurements with fibers in air and with fibers bonded to the Bragg gratings with epoxy).

Imec's process design kit (PDK) documentation is well established and it made our design based on imec's PDK an excellent teaching opportunity for our students at Koç University. Our students first learned the components, then they learned about the MPW tapeout process and then they learned about the details of the iSiPP50G PDK and designed the photonic circuit and analysed its performance under different device configurations.

In addition to imec's MPW runs, we are grateful to have received photonic and electronic packaging support from Tyndall National Institute, which has a routine design flow for imec MPW chips. Tyndall guided us in our design and relaxed some of their rules for our successful chip design, fabrication and packaging. Overall, without EUROPRACTICE bringing these PDKs, documentations and collaboration environment together, we would not be able to succeed in achieving our chip designs.

Acknowledgements

We acknowledge the support of Koç University via their high-performance computing and cloud storage infrastructure and services.

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Tunable LEDs for Integrated Photonics in Silicon (TuLIPS)

Delft University of Technology, the Netherlands

Contact:	Satadal Dutta
E-mail:	s.dutta-1@tudelft.nl
Technology:	imec Si-Photonics iSiPP50G
Die Size:	2.5mm x 2.5mm
Design Tools:	Synopsys Optodesigner
Application Area:	Agri-Food

Introduction

Efficient light-generation in standard silicon (Si) has been a key challenge for monolithic integration of photonic systems in CMOS technology. Despite its low optical power efficiency ($\eta \sim 10^{-6}$), electroluminescence (EL) from Si p-n junctions, in particular during avalanche-mode (AM) operation, has gained attention in recent years due to its broad-spectrum ($400 < \lambda < 900$ nm). This spectrum has a significant overlap with the responsivity of Si photodetectors (PDs), which has made the Si AM light-emitting diode (LED) a viable non-coherent light-source in monolithically integrated systems, *e.g.*, optical interconnects, micro-displays and pigment sensors. Nonetheless, it is highly desirable to increase η within a desired (narrow) range of $\Delta\lambda$ for such AMLEDs to boost the performance metrics of the aforesaid systems. In this paper we present our recent findings [1][2] on η-enhancement and λ-tuneability in AMLEDs and AM light-emitting transistor (LET). Specifically, we show the effect of Fabry-Pérot cavity resonances on the phonon-assisted hot carrier EL spectra, that occur during avalanche breakdown of Si p-n junctions.

Description

Micro-ring LEDs: Each Si micro-ring unit of radius R and width w consists of symmetrically doped half-rings, forming p-n junctions at two opposite ends (Fig. 1). Highly doped p+ and n+ implants offer ohmic contacts to metal layers routed to bond pads for biasing. For each LED, eleven such ring units are connected in parallel to increase the total device area, and thus light-output. The vertical SOI layer thickness post-fabrication is 0.21 µm. Design variations were included in R (0.6 – 2.0 µm), w (0.16 – 0.30 µm) and doping levels (lightly doped N1/P1 and highly doped N2/P2). The N1/P1 (N2/P2) LEDs show avalanche breakdown voltages (VBR) near −7 V (−14 V). The micro-rings emit light in AM operation (Fig. 1).

Avalanche-mode light-emitting transistor (AMLET): The AMLET consists of lateral n-p-n bipolar junctions with symmetrically doped emitter (E), base (B), and collector (C) regions (Fig. 2). The base length is 1.0 µm. The device is placed in a 21 µm x 10 µm Si island surrounded by SiO_2 on all faces.

Results

Micro-ring LEDs: AM-EL from each micro-ring LED was observed as localised bright twin spots from the p-n junctions (Fig. 1). The normalised spectral irradiance $\varepsilon(\lambda)$ of the ring LEDs with R=2.0 µm and w=0.3 µm are also shown. Irrespective of the doping level, two dominant narrow spectral bands were observed: $\lambda_{VIS} \approx 620$ nm with FWHM of 53 nm, and $\lambda_{NIR} \approx 764$ nm with FWHM of 66 nm. The relative intensities of these bands are 2-3 times higher than in prior reported Si AMLEDs. Further, the peak EL wavelengths λ_m of the ring LEDs in the 500 – 700 nm spectral range showed a consistent blue-shift with decreasing w.

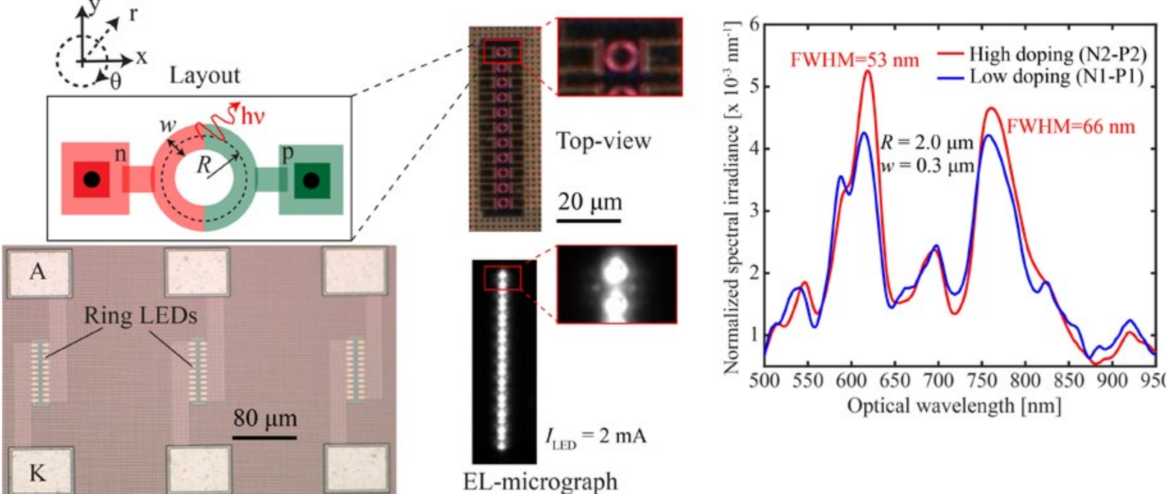

Fig.1: (Left) Schematic layout and die top-view of the micro-ring Si LEDs in the iSiPP50G technology. Also shown is the avalanche mode electroluminescent micrograph of a ring LED at the indicated bias. (Right) The normalized avalanche mode EL spectra of the ring LEDs of fixed geometry and different doping levels in their p-n junction. The spectra measured with an off-chip multi-mode fiber and spectrometer.

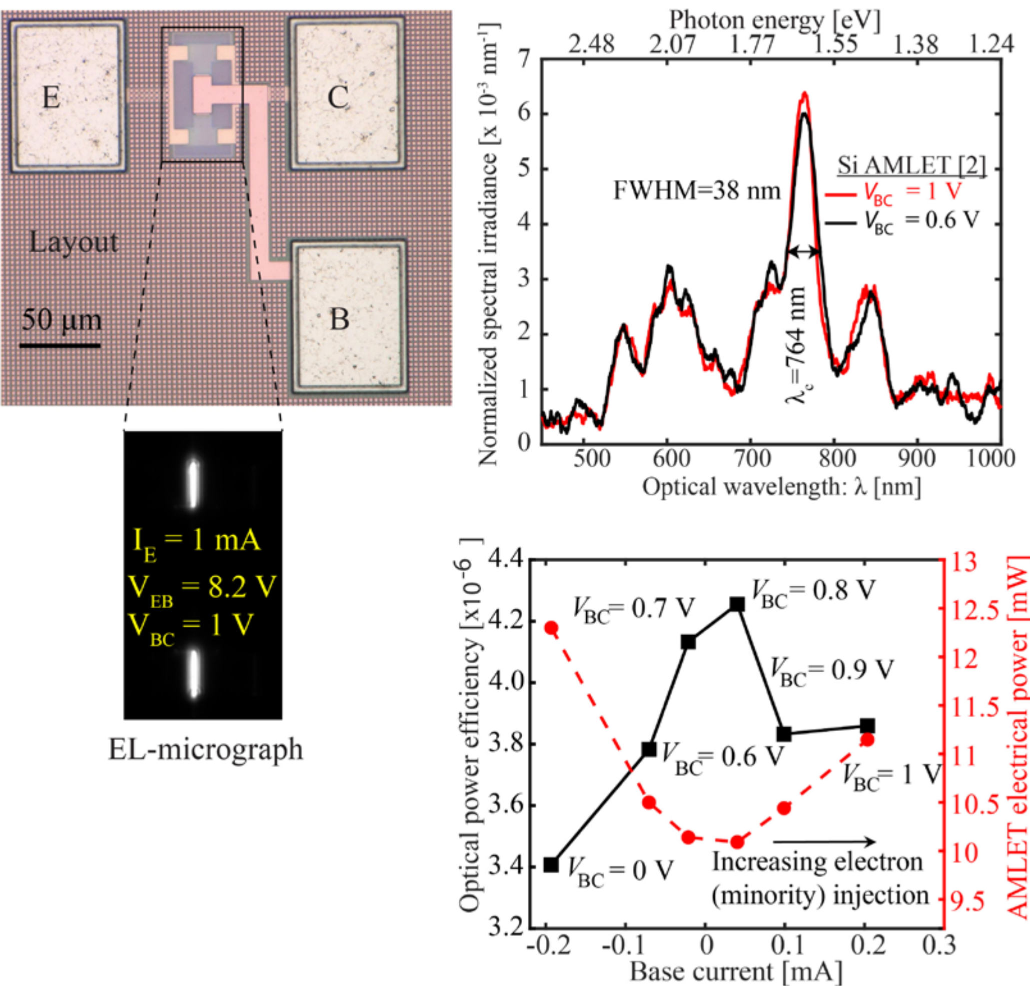

Fig.2: Device layout (top-view), AM EL micrograph, AM EL spectra (at indicated biases), measured optical power efficiency and electrical power consumption for the Si AMLET.

These results can be explained by FP resonances along the r-axis and z-axis of the Si cavity, where the $Si\text{-}SiO_2$ interfaces act as reflective boundaries. The calculated λ_m corresponding to integral resonance modes are in good agreement with the experiment. For a fixed ring geometry, the optical power efficiency (η_{opt} = P_{opt}/P_{LED}) was higher for the higher (N2/P2) doping level, due to the lower V_{BR} (and so, lower P_{LED}). Further, η_{opt} increased with decreasing R/w ratio (Fig. 2). A maximum η_{opt} = 3.2 x 10-5 at P_{LED} = 360 µW per p-n junction was obtained for R=0.6 µm and w=0.3 µm, a 1-order-of-magnitude improvement compared to that of state-of-the-art Si AMLEDs in various CMOS technologies.
AM light-emitting transistor (AMLET): The AMLET was measured in dc-operation at 298 K in common-base configuration. The E-B junction was set in avalanche mode to emit light (Fig. 2), whereas the B-C junction was forward biased in steps from 0 to 1 V, to inject minority carriers into the base. The AMLET EL spectrum showed three bands (Fig. 2): Y-band (λ= 600 nm), R-band (λ= 764 nm), and NIR band (λ= 850 nm). The R-band is significantly (2 times) brighter than the other bands. Further, the FWHM of the R-band is only 38 nm, with EL suppression in 650 – 700 nm λ-range, due to FP-resonance in the 0.21 µm thick SOI layer. As V_{BC} increased from 0 to 0.8 V, η_{opt} increased (Fig. 2) and reached a maximum at V_{BC}= 0.8 V.

Why EUROPRACTICE?

EUROPRACTICE offers access to the special imec Si photonics technology iSiPP50G, which was really the suitable platform to conduct my research on novel light emitters. EUROPRACTICE also offered us design tool license bundle at subsidised rates, for a smooth design process. The team provided technical know-how and aided us through the tapeout and other services. We were pleased with their service.

Acknowledgements

TU Delft: dr. W. Westerveld, dr. G.J. Verbiest, T. Erdogan; University of Twente: dr. ir. Raymond J.E. Hueting; 4TU Federation.

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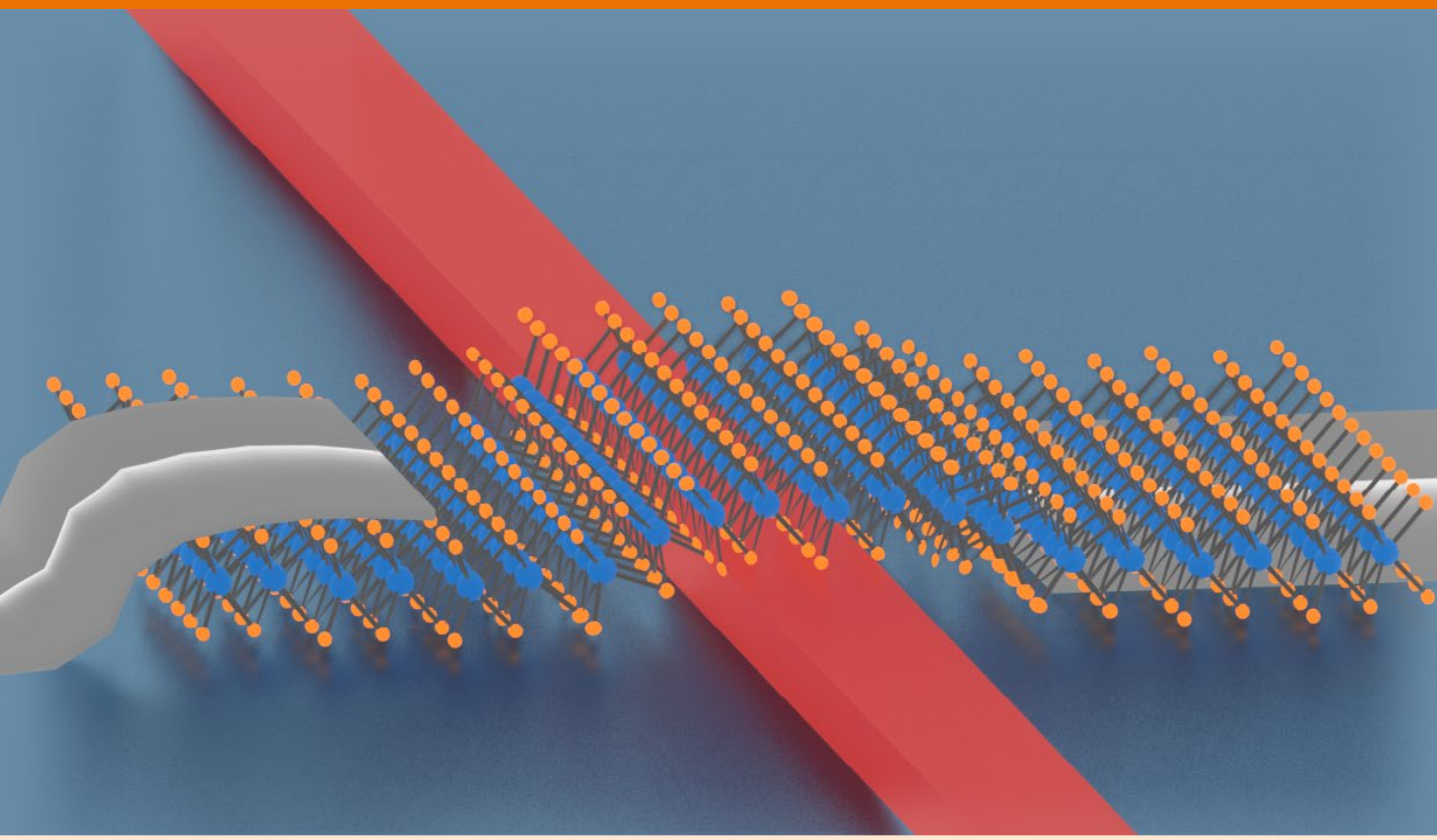

Fig.1: Sketch of the phase modulator based on atomically thin semiconductors.

Efficient modulators for silicon photonics

Nanophotonics Group, LMU Munich, Munich, Germany

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E-mails:	samarth.vadia@physik.uni-muenchen.de, j.foerste@physik.uni-muenchen.de
Technology:	CORNERSTONE Si-Photonics 220nm SOI
Die Size:	11470µm x 4900µm
Design Tools:	Luceda IPKISS, Ansys Lumerical
Application Area:	Computing & Quantum information processing

Introduction

Traditional approaches in photonics for controlling the phase of light fall short in providing an efficient and universal platform for programmable photonic circuits due to exhibiting certain limitations in technical requirements such as speed, energy consumption or losses. The lack of efficient modulator hinders the scalability of the photonic integrated circuits.

Description

Our project aims to establish two-dimensional materials as a viable tool for optical modulation via electrostatic doping to enable large-scale photonic integrated circuits with low-loss and high-speed next generation electro-optic modulators. In particular, we intend to combine atomically thin semiconductor transition-metal dichalcogenides, that provide efficient phase modulation with minimal absorption losses, with silicon photonics. The low-loss photonic integrated circuits with a large number of optical components are crucial for various applications, including communication, information processing, sensing and quantum technologies.

Why EUROPRACTICE?

EUROPRACTICE provides a consolidated platform for a range of services regarding IC development and prototyping. In particular, access to MPW services such as the one from open-source foundry CORNERSTONE is a great opportunity for academic and research institutions to pursue innovative high-risk projects in collaboration with a foundry.

Acknowledgements

We acknowledge the funding from Germany's Excellence Strategy Munich Center for Quantum Science and Technology (MCQST) EXC-2111-390814868.

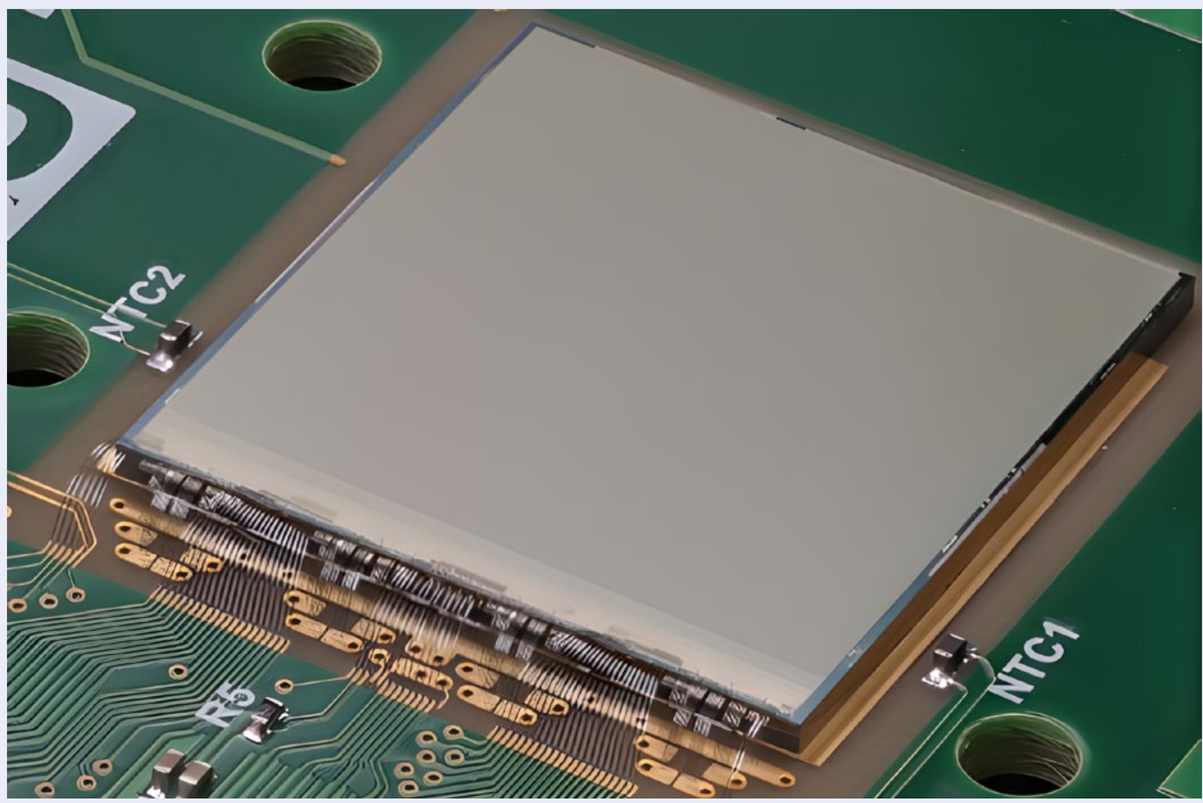

Fig.1: RD53 full sized pixel chip: 20mm x 20mm.

Pixel detector chip for extreme rates and radiation

CERN and RD53 Collaboration

Designers: RD53, collaboration of ~40 IC designers/students
E-mail: Jorgen.christiansen@cern.ch
Application Area: High Energy Physics (HEP)

RD53 Collaboration

The RD53 collaboration was established in 2013 to design hybrid pixel detector ASICs required for phase II upgrades of the ATLAS and CMS experiments in 2026, at the Large Hadron Collider (LHC) accelerator at CERN. Required to have significantly better spatial resolution with small pixels of 50µm x 50µm, extreme hit rate capability of up to 12 GHz per pixel chip, triggered event selection, high speed serial readout links (5 Gbits/s per chip) and novel serial powering for very low mass detector construction. Required to work reliably in extreme hostile radiation environment with up to 1Grad Total Ionising Dose (TID) and resilience to high rates of SEU/SET upsets, where pixel chips can have up to ~100 bit flips per second, induced by traversing high energy particles.

Developing the RD53 pixel chip

First years have been used to characterize the used TSMC 65nm technology for detailed radiation effects and determine how to design a pixel chip with extreme radiation tolerance (transistor layout and size, radiation simulations models) and required cold (-20 °C) operation to avoid detrimental annealing effects.

A large number of custom-made analog blocks have been specifically designed, prototyped and characterized for radiation tolerance (Pixel analog front-end, DAC, 12bit ADC, High speed PLL, link driver and receiver, serial power regulator, Bandgap, etc.). An optimized mixed signal architecture has been developed, with appropriately isolated analog islands with pixel analog front-ends embedded in a large digital sea of logic for charge digitization, data buffering and data assembly with programmable hit filtering with specific data compression for bandwidth efficient readout to DAQ. Digital architecture has been optimized for highly efficient use of TMR (Triple Modular Redundancy) in critical parts (~90% of design does not have TMR because of strict area and power constraints) and has been verified for correct function with extensive SEU injections. A first generation half sized chip was submitted in 2017, that has been extensively tested for analog and digital functions

and have been used for initial pixel detector system tests with bump-bonded pixel sensors and use of serial powered pixel modules with up to 48 pixel chips in an optimized serial/parallel powering chain configuration.
In 2020 full sized pixel chips with 150k pixels, for a total of ~500M transistors, have been submitted and extensively tested for correct function for TID and SEU/SET effects, supplemented with Ion, proton and laser testing to identify and resolve specific issues.

A large complex mixed signal pixel chip with 4 bit charge digitization on 150K pixels of 50µm x 50µm has been successfully developed, tested and qualified for extremely hostile radiation environments of up to 1Grad (factor 10.000 times higher than normally required for rad hard/tolerant space electronics).
Final production version chips for ATLAS and CMS upgrades will be submitted in 2023, for full scale production of ~50k pixel chips during the following two years.

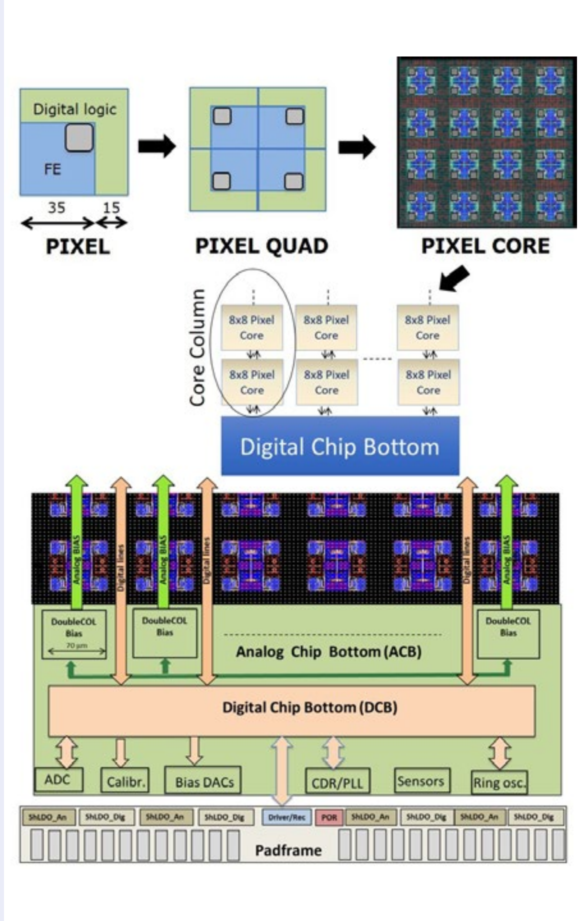

Fig.2: RD53 pixel chip implementation overview.

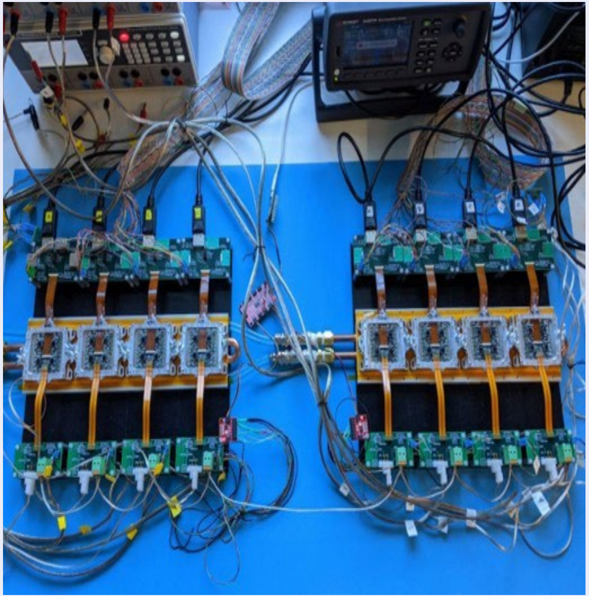

Fig.3: Pixel modules with 4 pixels chips per module being used in a serial power chain.

Why EUROPRACTICE?

The RD53 pixel chip development has been a very fruitful collaboration among 20 institutes across Europe (and US). This has to a very large extent been possible as required design and verification tools have been made available by EUROPRACTICE to a large distributed community of students and engineers in universities and physics research institutes.
The development of such complex ASICs requires the use of state-of-the-art EDA software tools for the design, the implementation and verification both at the component level as well as at the system level. EUROPRACTICE software service is an indispensable element for the ASIC developments at CERN and its collaborating institutes, supporting the use of a multitude of state-of-the-art EDA tools facilitating coherency in the collaborating design framework of distributed design teams.

Custom microelectronics components implemented in advanced technologies are vital parts of today's complex scientific instruments. The services provided by EUROPRACTICE allow a large community of physicists and engineers at CERN and in tens of collaborating Institutes working for these projects to use state-of-the-art EDA software tools and access advanced CMOS process for the construction of unique scientific instruments with a centralized high quality technical support.

More about RD53 Collaboration

RD53 public workshop and conference presentations: https://indico.cern.ch/category/5598/

RISC-V based open-source designs from PULP Platform

ETH Zurich and University of Bologna

Designers: The PULP team
E-mail: kgf@iis.ee.ethz.ch

Application Area: Processors, Open-Source Hardware

PULP platform

As this report goes to press, the Parallel Ultra Low Power (PULP) platform developed by ETH Zurich and University of Bologna will celebrate 10 years of working on open-source computing architectures that are based around the RISC-V architecture. Throughout this adventure, we have been involved in the design and test of more than 50 ASICs with the help of EUROPRACTICE and our designs have found wide-spread use both in academia and industry, thanks to the permissive licensing we have adopted for our designs.

We continue to use our designs for student projects, our own research, as well as industrial collaborations. The selection of ASICs were sent for manufacturing in 2021 and have been tested/evaluated in 2022.

One of the most important aspects of open-source hardware development has been that it has made SoC design more accessible for research and academic institutions as well as SMEs. In a modern SoC, large part of ASIC is typically occupied by a computing subsystem, and in many cases the innovative aspect of the design is confined to a relatively small (but still vital) part of the system. Being able to take, share, modify and adapt the basic computing platform from an open-source repository allows us (and hopefully other groups and companies) to develop ASICs that are more relevant and gives us more time to concentrate on parts of the design that make a difference and improve productivity. Each of the ASICs presented here rely for the large part on the RTL code published under the PULP platform GitHub page (https://github.com/pulp-platform) and builds on RISC-V based computing solutions.

Student projects

ETH Zurich has a very strong tradition in enabling students during their Bachelor/Master studies to work on actual integrated circuit design as part of a Bachelor/Semester thesis working in a group and supervised by experienced assistants.

Fig.1: Dogeram die.

Dogeram (TSMC65nm, 2mm x 1mm) is the result of such a student project where the main goal is to design and implement a Reduced Pin Count (RPC) DRAM interface from Etron Technology attaching it to a minimal PULP based system with two 32bit RISC-V cores called Snitch. This is the first silicon implementation of the RPC DRAM interface and has been successfully tested with actual RPC DRAM instances.

Fig.2: Minpool dies on the tray.

Another ASIC realized as part of a semester project is Minpool (TSMC65nm, 2.4mm x 2.4mm) uses the same Snitch cores but this time the innovation is to find efficient methods to allow multiple (in theory 100s of cores) processing cores to have low-latency access to local scratchpad memories of every processing cluster, effectively creating a pool of memory to be used by all participating cores. As a scaled down version of Mempool and Terapool architectures, Minpool still integrates 16 RISC-V cores and adds the necessary interfaces for debugging and communicating with the external world.

While the previous works were all 32bit RISC-V cores, Yun (TSMC65 2mm x 3mm) implements the CVA6 64-bit RISC-V core together with a matched four-lane vector unit called Ara including the debugging interface and support circuitry.

Fig.3: Yun die.

Research projects

Researchers at ETH Zurich and University of Bologna have collaborated on more ambitious research projects resulting in several additional ASICs in 2022 as well.

Zest (TSMC65, 4mm x 3mm) is a project that aims to bridge two different 32bit RISC-V based many-core architectures developed within PULP platform and features one cluster with eight CV32E40P cores and a second cluster with five Snitch cores adding an efficient peripheral system to allow all 13 cores to access a rich collection of interfaces including UART, I2C, QSPI, Hyperbus, interfaces for various frame and event-based cameras as well as a custom double data-rate serial interface.

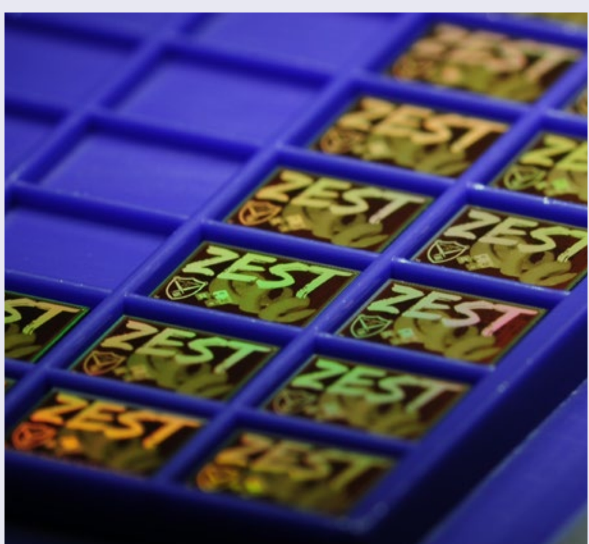

Fig.4: Zest dies on the tray.

Echoes (TSMC65 2mm x 2mm) goes another direction and implements a single 32bit CV32E40P RISC-V core around the PULPissimo microcontroller, adds an FFT accelerator and several I2C peripherals to allow it to retrieve and process audio signals from multiple sources.

Fig.5: Layout of Echoes.

Highlights

In terms of research impact, the most successful designs of our group from this period are Darkside and Kraken.

Darkside (TSMC65 4mm x 3mm) is a low-power RISC-V based heterogeneous IoT processor designed for TinyML DNN inference and on-chip training. The main computing unit is a cluster with eight RISC-V cores, enhanced to be able to operate with 2–32-bit mixed-precision integer SIMD instructions and fused MAC-load operations. It also features specialized accelerators to boost the performance of integer depthwise convolutions, reduce the latency of data marshalling operations, and enhance the performance and efficiency of FP16 kernels. Measurement results showed a maximum operating frequency of 290MHz (at 1.2V) and showed a peak efficiency of 835 GOPS/W when executing typical on ML workloads. In addition, Darkside also includes a novel SRAM memory macro designed by the Embedded Systems Laboratory of EPFL to support in-memory computing operations.

Using a more advanced 22nm FDSOI technology, Kraken (GF22, 3mm x 3mm) is also designed as an eight+one core IoT processor with three dedicated accelerators. The first

Fig.6: Darkside die.

accelerator is called CUTIE (Completely Unrolled Ternary Inference Engine) and has been optimized to be used for ternary CNN applications achieving an impressive 1036 TOp/s/W peak efficiency when coupled with aggressive voltage scaling offered by the technology. The second accelerator has been designed to work in concert with event-based sensors and specifically image sensors. The Sparse Neural Engine (SNE) is able to accelerate spiking neural network (SNN) inference tasks by exploiting the implicit temporal/spatial location encoding of input-events achieving 51.2 HSOP/s and an energy efficiency of 4.5TSOP/s/W. The third accelerator has been contributed by the Integrated Information Processing (IIP) group of ETH Zurich led by Prof. Christoph Studer and is a floating-point baseband accelerator called PULPO that is tightly integrated within the datapath of the 8-core computing cluster of Kraken and has been designed to support operations for massive MU-MIMO within base stations.

Finally, Marsellus (GF22 4mm x 3mm) is an excellent example of industry cooperation. Designed together with Dolphin Design, it is based around our many-core 32bit RISC-V processor systems and features sixteen RISC-V cores and achieves 12.4TOPS/W efficiency.

Why open-source hardware?

One of the most underrated parts of our work is how much open-source hardware principles have fostered cooperation and design reuse. The eight designs presented here include more than 64 RISC-V processors based on three different RISC-V processor families (CVA6, CV32E40P, Snitch) and their supporting infrastructure. Several of the works contributed to enhancements to existing systems (Dogeram, Yun, Minpool, Zest) while others were based on tried and verified designs and were able to concentrate on specific application domains (Audio, Spiking Neural Networks, Baseband processing, TinyML), most of these designs included close cooperations with various research groups and industry. As we compile this report, the next-generation designs are already underway and we look forward to describing the results in the upcoming years.

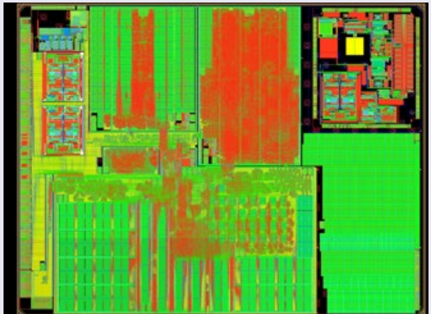

Fig.8: Layout of Marsellus.

Fig.7: Application board using the Kraken chip connected to an event-based camera system.

Why EUROPRACTICE?

For an academic institution, designing a complex SoC is quite a challenging task. Accomplishing to tapeout several ASICs and being able to successfully test and evaluate them in a year is only possible if you get excellent supporting partners. EUROPRACTICE has been an indispensable help for obtaining the licenses for the EDA design flows needed as well as the MPW services by EUROPRACTICE. Their help goes much beyond IC submission: They also help us navigate tricky problems, help us with packaging solutions as well as make us aware of different implementation options and ensure that our submissions to the foundries are devoid of critical DRC errors.

More about PULP

PULP team: .... pulp-platform.org/team.html
PULP platform GitHub page: . github.com/pulp-platform
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Acknowledgements

Several of these designs have been supported in part through funds from various EU Horizon projects, Ampere (#871669), Fractal (#877056), Oprecomp (#732631), Wiplash(#863337), the European Processor Initiative, OpenHW group, the Swiss National Science Foundation and Armasuisse Science and Technology.

Publications

M. Scherer, A. Di Mauro, G. Rutishauser, T. Fischer and L. Benini, "A 1036 TOp/s/W, 12.2 mW, 2.72 μJ/Inference All Digital TNN Accelerator in 22 nm FDX Technology for TinyML Applications," 2022 IEEE Symposium in Low-Power and High-Speed Chips (COOL CHIPS), 2022, pp. 1-3, doi: 10.1109/COOLCHIPS54332.2022.9772668.

Garofalo et al., "Darkside: 2.6GFLOPS, 8.7mW Heterogeneous RISC-V Cluster for Extreme-Edge On-Chip DNN Inference and Training," ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC), 2022, pp. 273-276, doi: 10.1109/ESSCIRC55480.2022.9911384.

Garofalo et al., "DARKSIDE: A Heterogeneous RISC-V Compute Cluster for Extreme-Edge On-Chip DNN Inference and Training," in IEEE Open Journal of the Solid-State Circuits Society, vol. 2, pp. 231-243, 2022, doi: 10.1109/OJSSCS.2022.3210082.

M. Scherer, G. Rutishauser, L. Cavigelli and L. Benini, "CUTIE: Beyond PetaOp/s/W Ternary DNN Inference Acceleration With Better-Than-Binary Energy Efficiency," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 41, no. 4, pp. 1020-1033, April 2022, doi: 10.1109/TCAD.2021.3075420.

Di Mauro, A. S. Prasad, Z. Huang, M. Spallanzani, F. Conti and L. Benini, "SNE: an Energy-Proportional Digital Accelerator for Sparse Event-Based Convolutions," 2022 Design, Automation & Test in Europe Conference & Exhibition (DATE), 2022, pp. 825-830, doi: 10.23919/DATE54114.2022.9774552.

O. Castañeda, L. Benini and C. Studer, "A 283 pJ/b 240 Mb/s Floating-Point Baseband Accelerator for Massive MU-MIMO in 22FDX," ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC), 2022, pp. 357-360, doi: 10.1109/ESSCIRC55480.2022.9911311.

M. Scherer, A. D. Mauro, T. Fischer, G. Rutishauser and L. Benini, "TCN-CUTIE: A 1036 TOp/s/W, 2.72μJ/Inference, 12.2 mW All-Digital Ternary Accelerator in 22 nm FDX Technology," in IEEE Micro, doi: 10.1109/MM.2022.3226630.

F. Conti, D. Rossi, G. Paulin, A. Garofalo, A. Di Mauro, G. Rutishauer, G. Ottavi, M. Eggimann, H. Okuhara, V. Huard, O. Montfort, L. Jure, N. Exibard, P. Gouedo, M. Louvat, E. Botte, L. Benini, "A 12.4TOPS/W @ 136GOPS AI-IoT System-on-Chip with 16 RISC-V, 2-to-8b Precision-Scalable DNN Acceleration and 30%-Boost Adaptive Body Biasing", accepted for publication at IEEE International Solid State Circuits Conference 2023.

EUROPRACTICE MEMBERSHIP

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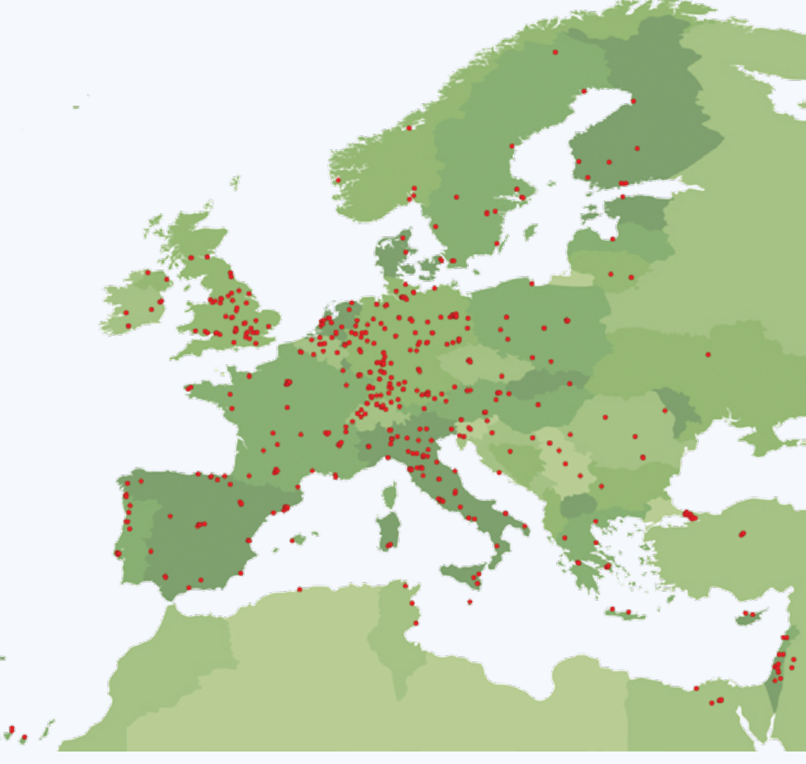

Together with the funding provided by the European Commission, EUROPRACTICE needs additional support to provide high quality service to more than 600 European universities and research institutes. Membership Fees pay for extra staff supporting this requested stimulation activity for academic institutions (not fully paid by the EC). The annual Membership Fee is collected by STFC on behalf of the EUROPRACTICE project partners.

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A35400	Hochschule Ulm
A35420	Georg-Simon-Ohm Hochschule Nürnberg
A35430	Karlsruher Institut für Technologie
A35450	Technische Universität Darmstadt - Integrierte Elektronische Systeme (IES)
A35500	Eberhard Karls Universität Tübingen
A35590	Johannes-Wolfgang-Goethe-Universität Frankfurt am Main
A35600	Technische Universität Carolo-Wilhelmina zu Braunschweig
A35620	Universität Bremen - Institut für Theoretische Elektrotechnik und Mikroelektronik
A35710	Hochschule Augsburg
A35810	Rheinland-Pfälzische Technische Universität Kaiserslautern-Landau
A35830	Universität Hamburg
A35990	Universität Duisburg-Essen
A36070	Carl von Ossietzky Universität Oldenburg - Informatik
A36440	Universität des Saarlandes
A37090	Technische Universität Dortmund
A37240	Hochschule Furtwangen
A37290	Leibniz Universität Hannover
A37310	Technische Universität Berlin
A37380	Friedrich-Alexander-Universität Erlangen-Nürnberg
A37390	Technische Universität München - Fakultät für Elektrotechnik und Informationstechnik München
A37440	Universität der Bundeswehr München
A37450	Hochschule Esslingen
A37500	Universität Paderborn
A37510	Hochschule für Angewandte Wissenschaften München
A37530	Humboldt-Universität zu Berlin
A37540	Universität Ulm
A37760	Technische Universität Dresden
A37800	Hochschule Offenburg
A37810	Rheinisch-Westfälische Technische Hochschule Aachen - Fakultät für Elektrotechnik und Informationstechnik
A37880	Hochschule Aalen
A37920	Hochschule Ravensburg-Weingarten
A37930	Hochschule Mannheim
A38010	Hochschule Heilbronn
A38030	Hochschule Darmstadt
A38080	Ruhr-Universität Bochum
A38090	Otto-von-Guericke-Universität Magdeburg
A38220	Universität Siegen
A38240	Technische Universität Ilmenau
A38340	Technische Universität Chemnitz

A38550	Ostfalia Hochschule für angewandte Wissenschaften
A38650	Fachhochschule Dortmund
A38890	Rheinische Friedrich-Wilhelms-Universität Bonn
A38940	Ernst-Abbe-Fachhochschule Jena
A39000	Technische Hochschule Mittelhessen - Gießen
A39070	Hochschule Karlsruhe - University of Applied Sciences
A39110	Universität Stuttgart
A39220	Universität Rostock
A39250	Ruprecht-Karls-Universität Heidelberg - ASIC
A39260	Albert-Ludwigs-Universität Freiburg
A39330	Hochschule Reutlingen
A39340	Martin-Luther-Universität Halle-Wittenberg
A39460	Christian-Albrechts-Universität zu Kiel
A39580	Hochschule Osnabrück
A39660	Friedrich-Schiller-Universität Jena
A39770	Universität zu Lübeck
R00150	Max-Planck-Institut für Physik
R20300	Institut für Mikroelektronik- und Mechatronik - Systeme gemeinnützige GmbH
R20330	Deutsches Elektronen-Synchrotron
R20460	Institut für Mobil- und Satellitenfunktechnik GmbH
R20510	IHP GmbH - Leibniz-Institut für innovative Mikroelektronik
R20570	Fraunhofer-Institut für Techno- und Wirtschaftsmathematik
R20720	DLR Institute of Systems Engineering for Future Mobility
R20880	GSI Helmholtzzentrum für Schwerionenforschung GmbH
R20890	Fraunhofer-Institut für Siliziumtechnologie
R20920	Fraunhofer-Institut für Integrierte Schaltungen - Erlangen
R20930	Fraunhofer-Institut für Integrierte Schaltungen - Dreden
R21050	Max-Planck-Institut für Chemie
R21060	Forschungszentrum Jülich
R21090	Fraunhofer Heinrich-Hertz-Institut
R21120	Max-Planck-Institut für extraterrestrische Physik
R21150	Physikalisch-Technische Bundesanstalt - Braunschweig
R21220	Fraunhofer-Institut für Integrierte Systeme und Bauelementetechnologie
R21260	Hochschule für Technik und Wirtschaft Dresden
R21310	Fraunhofer-Institut für Photonische Mikrosysteme
R21320	Fraunhofer-Institut für Solare Energiesysteme
R21510	Deutsches Zentrum für Luft- und Raumfahrt - Berlin
R21530	Deutsches Zentrum für Luft- und Raumfahrt - Bremen
R21580	Deutsches Zentrum für Luft- und Raumfahrt IIP - Berlin
R21610	Helmholtz-Zentrum Berlin für Materialien und Energie
R21620	Fraunhofer-Einrichtung für Angewandte und Integrierte Sicherheit
R21630	Fraunhofer-Institut für Zerstörungsfreie Prüfverfahren
R21650	Fraunhofer-Institut für Hochfrequenzphysik und Radartechnik
R21770	Konrad-Zuse-Zentrum für Informationstechnik Berlin
R21780	Deutsches Zentrum für Luft- und Raumfahrt - Wessling
R21790	NaMLab gGmbH
R21900	Max-Planck-Institut für Radioastronomie
R21970	PNSensor gGmbH
R22020	European XFEL
R22080	Fraunhofer Institute for Organic Electronics, Electron Beam and Plasma Technology FEP
R22110	Physikalisch-Technische Bundesanstalt - Berlin
R22150	Fraunhofer Institute SIT
R22160	Halbleiterlabor der Max Planck Gesellschaft
R22260	Helmholtz-Zentrum Geesthact
R22290	Fraunhofer-Einrichtung für Mikrosysteme und Festkörper-Technologien EMFT
R22340	Optotransmitter-Umweltschutz-Technologie e.V
R22370	CIS Forschungsinstitut fuer Mikrosensorik GmbH
R22440	Hahn-Schickard-Gesellschaft fuer Angewandte Forschung e.V.
R22500	Max-Planck-Institut für Mikrostrukturphysik
R22530	European Molecular Biology Laboratory
R22650	Max-Planck-Institute for Software Systems

Code	Institution
R22670	Institut für Mikroelektronik Stuttgart
R22710	Fraunhofer Institut fuer Mikroelektronische Shaltungen und Systeme (IMS)
R22770	CISPA-Helmholtz-Zentrum Fur Informaitonssicherheit gGmbH
R22840	Ferdinand-Braun-Institut gGmbH
R22860	German Aerospace Center (DLR) - Galileo Competence Center
R22910	Barkhausen Institut

Ghana

Code	Institution
A14770	Kwame Nkrumah University of Science & Technology

Greece

Code	Institution
A00530	University of Ioannina
A13550	University of Thessaly
A14150	Athens University of Economics and Business
A14700	University of Piraeus
A16720	National and Kapodistrian University of Athens
A16850	University of the Peloponnese
A35140	National Technical University of Athens
A35960	University of Patras - Electrical and Computer Engineering
A37550	National and Kapodistrian University of Athens
A37680	University of Patras
A39280	Aristotle University of Thessaloniki
A39490	Technical University of Crete
R20790	Demokritos, National Center for Scientific Research
R21080	Foundation for Research and Technology Hellas
R22640	Athena Research Centre

Hungary

Code	Institution
A40010	Budapesti Muszaki és Gazdaságtudományi Egyetem
A47540	Pázmány Péter Katolikus Egyetem

Ireland

Code	Institution
A01190	Munster Technological University
A13410	Institute of Technology, Carlow
A15730	University College Dublin
A35300	University College Cork
A36510	University of Limerick
A39310	Technological University Dublin, Tallaght Campus
R21720	Tyndall National Institute
R22400	Dublin Institute for Advanced Studies

Israel

Code	Institution
A13240	The Hebrew University of Jerusalem
A13330	Technion - Israel Institute of Technology
A13910	Ben-Gurion University of the Negev
A13920	Bar-Ilan University
A14070	Ort Braude College of Engineering
A14380	Tel-Aviv University
A14540	Kinneret College on the Sea of Galilee
A14690	Holon Institute of Technology
A15190	Jerusalem College of Technology

Italy

Code	Institution
A00120	Università Politecnica delle Marche
A00520	Università degli Studi di Modena e Reggio Emilia - Modena
A00560	Università degli Studi di Siena
A00680	Università della Calabria
A00740	Università degli Studi di Perugia
A12000	Università di Bologna - DEIS
A12370	Università degli Studi di Napoli Federico II - DIETI
A12390	Università degli Studi di Brescia
A12530	Università degli Studi di Verona
A12640	Università degli Studi di Milano
A12770	Università del Salento
A12990	Università degli Studi di Bergamo
A13280	Università degli Studi di Udine
A14220	Università degli Studi di Trento
A14800	Università degli Studi di Milano-Bicocca
A14820	Università degli Studi di Salerno
A14860	Università degli Studi di Modena e Reggio Emilia - Reggio Emilia
A15070	Scuola Superiore di Studi Universitari e di Perfezionamento Sant'Anna
A15750	Università Degli Studi di Cassino e del Lazio Meridionale
A15900	Università di Bologna - Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi" (Cesena)
A16130	Università degli Studi Roma Tre
A16460	Politecnico di Bari
A16570	University of Bologna
A16800	Universita Degli Studi Di Firenze
A35210	Università degli Studi di Parma
A35530	Politecnico di Torino
A35550	Università degli Studi di Roma Tor Vergata
A35660	Università di Pisa
A35690	Politecnico di Milano
A35910	Università degli Studi di Genova
A36380	Università di Bologna - Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi" (Bologna)
A37280	Università degli Studi di Pavia
A37460	Università degli Studi di Catania
A38380	Politecnico di Bari
A38620	Università degli Studi di Torino
A38840	Università degli Studi di Roma "La Sapienza"
A39200	Università degli Studi di Padova
A39410	Università degli Studi dell'Aquila
A39550	Università degli Studi di Firenze
A39570	Università degli Studi di Cagliari
R00140	Fondazione Bruno Kessler
R00270	Istituto Nazionale di Fisica Nucleare, Sezione di Genova
R00300	Istituto Nazionale di Fisica Nucleare, Sezione di Pisa
R20310	Istituto Nazionale di Fisica Nucleare, Sezione di Roma
R20320	Istituto Nazionale di Fisica Nucleare, Sezione di Roma II
R20400	Istituto Nazionale di Fisica Nucleare, Sezione di Bologna
R20420	Istituto Nazionale di Fisica Nucleare, Sezione di Trieste
R20440	Istituto Nazionale di Fisica Nucleare, Sezione di Torino
R20450	Istituto Nazionale di Fisica Nucleare, Laboratori Nationali di Frascati
R20470	Istituto Nazionale di Fisica Nucleare, Sezione di Padova
R20550	Elettra-Sincrotrone Trieste
R20630	Istituto Nazionale di Fisica Nucleare, Sezione di Milano
R20670	Istituto Nazionale di Fisica Nucleare, Sezione di Cagliari
R20710	Istituto Nazionale di Fisica Nucleare, Sezione di Bari
R20990	Istituto Nazionale di Fisica Nucleare, Sezione di Ferrara
R21100	Istituto Nazionale di Fisica Nucleare, Sezione di Napoli
R21160	Istituto Nazionale di Astrofisica, Osservatorio Astrofisico di Arcetri
R21190	Istituto Nazionale di Fisica Nucleare, Laboratori Nationali del Gran Sasso
R21300	Consiglio Nazionale delle Richerche, Istituto per la Microelettronica e i Microsistemi
R21450	Istituto Nazionale di Fisica Nucleare, Sezione di Pavia
R21570	Istituto Nazionale di Astrofisica, Istituto di Radioastronomia
R21600	Istituto Italiano di Technologia
R21760	Consiglio Nazionale delle Richerche, Istituto per la Microelettronica e i Microsistemi Catania
R21800	Consiglio Nazionale delle Richerche, Istituto per la Microelettronica e i Microsistemi Roma
R21940	The Abdus Salam International Centre for Theoretical Physics
R22010	Istituto Nazionale di Astrofisica Osservatorio Astronomico di Cagliari

R22070 Instituto per lo Studio dei Materiali Nanostrutturati
R22120 Istituto Nazionale di Astrofisica - Istituto di Radioastronomia - Radiotelescopi di Medicina
R22200 Radio Analog Micro Electronics srl
R22390 Instituto Nazionale di Fisica Nucleare Sezione di Perugia
R22450 European Gravitational Observatory
R22490 Istituto Nazionale di Fisica Nucleare
R22550 Consorzio Nazionale Interuniversitario per le Telecomunicazioni
R22790 Instituto Nanoscienze - CNR

Jordan

A15990 Princess Sumaya University for Technology
A16140 Jordan University of Science & Technology

Kazakhstan

A48080 Nazarbayev University

Kuwait

A16820 Kuwait College of Science and Technology

Latvia

A48060 Riga Technical University

Lebanon

A47650 American University of Beirut
R22630 Houmal Technology Park

Lithuania

A40230 Kauno Technologijos Universitetas
A47980 Vilniaus Universitetas
A48050 Vilniaus Gedimino Technikos Universitetas
R49200 Baltic Institute of Advanced Technology (BPTI)

Luxembourg

A15780 Université du Luxembourg

Malta

A38720 University of Malta

Norway

A12750 Universitetet i Sørøst-Norge
A37360 Universitetet i Oslo
A37560 Norges Teknisk Naturvitenskapelige Universitet - Institutt for elektroniske systemer
A37820 Universitetet i Bergen
R21460 SINTEF Stiftelsen for industriell og teknisk forskning

Palestine

A16240 Birzeit University
A16370 An-Najah National University

Poland

A40100 Uniwersytet Zielonogórski
A40120 Politechnika Warszawska
A40130 Politechnika Lódzka - Mikroelektroniki I Technik Informatycznych (DMCS)
A40140 Akademia Górniczo-Hutnicza im. Stanislawa Staszica
A40160 Politechnika Wroclawska
A40530 Politechnika Slaska
A47300 Politechnika Gdanska
A47400 Politechnika Poznanska - Inzynierii Komputerowej
A47670 Politechnika Poznanska - Radiokomunikacji
A47740 Politechnika Lódzka - Pólprzewodnikowych I Optoelektronicznych
A48230 Rzeszow University of Technology
R22610 Institute of High Pressure Physics (UNIPRESS)
R40030 Siec Badawcza Lukasiewicz - Instytut Mikroelektroniki I Fotoniki
R49030 Instytut Podstawowych Problemów Techniki PAN (IPPT-PAN)
R49080 Centrum Badan Kosmicznych PAN

Portugal

A12310 Universidade Nova de Lisboa
A12550 Universidade do Minho
A13710 Instituto Superior de Engenharia de Lisboa
A35540 Universidade do Porto
A35670 Universidade de Aveiro
A35970 Instituto Superior Técnico
A37230 Instituto de Engenharia de Sistemas e Computadores - Investigação e Desenvolvimento
R14120 Instituto de Telecomunicações - Lisboa
R21710 Laboratório de Instrumentação e Física Experimental de Partículas
R21750 International Iberian Nanotechnology Laboratory
R21890 Instituto de Telecomunicações - Aveiro
R22170 Instituto de Sistemas Robótica (ISR-UC)

Romania

A15520 Universitatea Politehnica din Bucuresti
A15560 Universitatea Tehnică "Gheorghe Asachi" din Iași
A16070 Universitatea Transilvania Brasov
A47880 Universitatea Politehnica din Timișoara
A48070 Universitatea Tehnica din Cluj-Napoca
R49010 Institutul National pentru Fizica si Inginerie Nucleara - Horia Hulubei - Nuclear Hadrons
R49060 Institutul National pentru Fizica si Inginerie Nucleara - Horia Hulubei - Particle Physics

Serbia

A47510 Univerzitet u Nišu
A47600 Univerzitet u Novom Sadu
A48010 Univerzitet u Beogradu
A48170 Univerzitet u Kragujevcu
A48200 Univerzitet u Novom Sadu
R49230 BioSense Institute

Slovakia

A40050 Slovenská technická univerzita v Bratislave
A47930 Technická univerzita v Kosiciach

Slovenia

A40280 Univerza v Ljubljani
A47690 Institut "Jozef Stefan"
A47820 Univerza v Mariboru
R22580 Skylabs Vesoljske Tehnologije Doo

South Africa

A14560 University of Pretoria

Spain

A12320 Universidad Politécnica de Cartagena
A12590 Universidad de Castilla - La Mancha
A13150 Universitat de València
A13340 Universidad de Alcalá
A13860 Universidad de Salamanca
A14720 Universidad de La Laguna
A15370 Universidad de Deusto
A16290 Universitat Pompeu Fabra
A16340 University of Vigo - AtlanTTic
A35130 Universidad Politécnica de Madrid - Departamento de Ingeniería Electrónica
A35190 Universitat Politècnica de València
A35870 Universidad de Sevilla - Instituto de Microelectrónica de Sevilla (IMSE-CNM)
A35891 Universidad de Cantabria
A36250 Universitat Autònoma de Barcelona
A36390 Universidad de Las Palmas de Gran Canaria - Instituto Universitario de Microelectrónica Aplicada (IUMA)

A37060	Universidad de Zaragoza - Dpto.Ingenieria Electronica y Comunicaciones
A37080	Universidad de Santiago de Compostela
A37330	Universidad Complutense de Madrid
A37580	Universidad de Malaga
A37690	Universidad del Pais Vasco
A38330	Universidad de Vigo
A38360	Universitat de les Illes Balears
A38580	Universidad de Sevilla - Ingenieria Electronica
A38590	Universidad de Granada
A38600	Universidad de Navarra
A38660	Universitat de Barcelona
A38780	Universidad de Las Palmas de Gran Canaria - Departamento de Informàtica y Sistemas
A38790	Universidad de Zaragoza - Facultad de Ciencias
A38820	Universidad Politécnica de Madrid - Centro de Electrónica Industrial
A39080	Universidad de Extremadura
A39100	Universidad Pública de Navarra
A39150	Universitat Politècnica de Catalunya - Departamento de Ingeniería Electrónica (Campus Nord)
A39180	Universitat Rovira i Virgili
A39390	Universitat Autónoma de Madrid
A39540	Universidad Carlos III de Madrid
R00060	CNM - Instituto de Microelectrónica de Barcelona
R20700	Ikerlan
R20850	Centre Tecnològic de Telecomunicacions de Catalunya
R21230	Instituto de Fisica Corpuscular
R21520	Institute of Space Sciences (ICE-CSIC)
R21550	Institut de Ciències Fotòniques
R21740	Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas
R21910	Instituto de Tecnologías Físicas y de la Información
R22100	Centro Nacional de Supercomputación, Barcelona
R22460	Consorcio ESS Bilbao
R22470	Asociacion Centro Tecnológico
R22600	Centro Tecnológico de Automoción de Galicia
R22700	Instituto de Astrofisica de Canarias
R22750	Institut De Fisica D'Altes Energies (IFAE)
R22870	Instituto Tecnologico de Aragon - ITAINNOVA
R22880	CIC nanoGUNE
R22890	Centro Nacional de Aceleradores

Sweden

A00260	Luleå tekniska universitet
A13720	Uppsala universitet
A16360	Kungliga Tekniska Hogskolan, Stockholm
A16730	Linnéuniversitetet
A16760	Uppsala universitet
A16860	Karlstads universitet
A37350	Linköpings universitet
A37370	Lunds universitet
A38180	Kungliga Tekniska högskola, Kista
A38670	Chalmers Tekniska högskola
A39840	Mittuniversitetet
R20690	Research Institutes of Sweden, ICT Acreo
R20910	Totalförsvarets forskningsinstitut FOI
R21990	European Spallation Source
R22050	Institutet för Rymdfysik

Switzerland

A05000	Scuola Universitaria Professionale della Svizzera Italiana
A12920	Universität Zürich
A13090	Università della Svizzera Italiana
A13630	Université de Genève
A14780	Haute école d'ingénierie et d'architecture Fribourg
A15480	Universität Basel
A15530	Universität Bern
A16440	Universität Zurich
A36110	École Polytechnique Fédérale de Lausanne - Microelectronics Systems
A37340	École Polytechnique Fédérale de Lausanne - Neuchâtel
A38100	Ostschweizer Fachhochschule
A38310	Eidgenössische Technische Hochschule Zürich
A38410	Berner Fachhochschule
A38800	Eidgenössische Technische Hochschule Zürich - Basel
A39820	University of Applied Sciences and Arts Northwestern Switzerland
R20350	Organisation Européenne pour la Recherche Nucléaire
R20680	Centre Suisse d'Electronique et Microtechnique - Neuchâtel
R20800	Paul Scherrer Institut
R20970	Centre Suisse d'Electronique et Microtechnique - Zürich

The Netherlands

A00170	Universiteit Twente - CAES
A12010	Vrije Universiteit Amsterdam
A12650	Radboud Universiteit Nijmegen
A13730	Stichting Saxion
A14510	Rijksuniversiteit Groningen
A15420	Erasmus Universitair Medisch Centrum Rotterdam
A15960	Universiteit van Amsterdam
A16770	Universiteit Leiden
A35701	Technische Universiteit Delft
A38050	Technische Universiteit Eindhoven
R00280	Nikhef
R20370	TNO-FEL
R20430	European Space Agency - ESTEC Microelectronics
R20520	Stichting Nederlandse Wetenschappelijk Onderzoek Instituten / Stichting ASTRON, Netherlands Institute for Radio Astronomy
R20540	European Space Agency - ESTEC Payload Technology
R21200	Stichting imec Nederland
R21250	NWO-I/SRON

Tunisia

A12930	École Nationale d'ingénieurs de Sfax
A15300	École Nationale d'ingénieurs de Tunis
R22570	Center for Research in Microelectronics and Nanotechnology

Turkey

A13010	Sabanci Üniversitesi
A13530	TC Kocaeli Üniversitesi
A13820	Koc Universitesi
A14250	Yeditepe Üniversitesi
A14730	TOBB Ekonomi ve Teknoloji Üniversitesi
A15280	Orta Dogu Teknik Üniversitesi Kuzey Kibris Kampusu
A15680	Ankara Yildirim Beyazit Üniversitesi
A15870	Istanbul Bilgi Üniversitesi
A15970	Özyegin Üniversitesi
A16250	Istanbul Medipol Üniversitesi
A16550	Maltepe University
A16660	Atilim University
A16750	Gebze Teknik Üniversitesi
A37960	Istanbul Teknik Üniversitesi
A38270	Ihsan Dogramaci Bilkent Üniversitesi
A38440	Orta Dogu Teknik Üniversitesi
A39170	Bogaziçi Üniversitesi
R22740	TUBITAK - UME (National Metrology Institute of Turkey)
R38860	Türkiye Bilimsel ve Teknik Arastirma Kurumu -BILGEM

	UK
A12480	University of Bath
A13480	Imperial College London
A13490	King's College London
A13510	Royal Holloway University of London
A13520	University College London
A13620	University of Manchester Jodrell Bank Observatory
A14580	University of Lincoln
A14750	UCL Mullard Space Science Laboratory
A15390	The Open University
A15450	Cardiff University
A15790	City University London
A16000	Coventry University
A16050	Cranfield University
A16580	University of Chester
A35030	Sheffield Hallam University
A35080	University of Manchester
A35111	University of Sussex
A35180	University of Nottingham
A35330	Newcastle University
A35410	University of Hull
A35440	University of Essex
A35470	University of Sheffield
A35520	Northumbria University
A35780	University of Cambridge
A36000	University of Bristol
A36090	University of Ulster
A36120	University of Strathclyde
A36280	Brunel University
A36341	University of Liverpool
A36342	Liverpool John Moores University
A37300	University of Birmingham
A37320	University of Oxford
A37400	University of Huddersfield
A37420	University of Edinburgh
A37430	University of the West of England
A37490	Queen's University of Belfast
A37570	University of Surrey
A37600	University of Hertfordshire
A37610	University of Southampton
A37630	University of Warwick
A37730	University of Leeds
A37780	University of South Wales
A37840	University of Durham
A37870	Swansea University
A37900	Manchester Metropolitan University
A38450	Loughborough University
A38810	University of York
A39440	University of Glasgow
A39650	University of Salford
R00050	STFC Rutherford Appleton Laboratory
R20600	STFC Daresbury Laboratory
R20950	Diamond Light Source
R22030	STFC UK Astronomy Technology Centre
R22090	Culham Centre for Fusion Energy
	Ukraine
A47610	National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute"
	Uzbekistan
A16380	Urganch State University
A16390	Andizhan State University
A48190	Tashkent University of Information Technologies

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E-Mail: MicroelectronicsCentre@stfc.ac.uk

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Tel: +44 (0) 1235 445327
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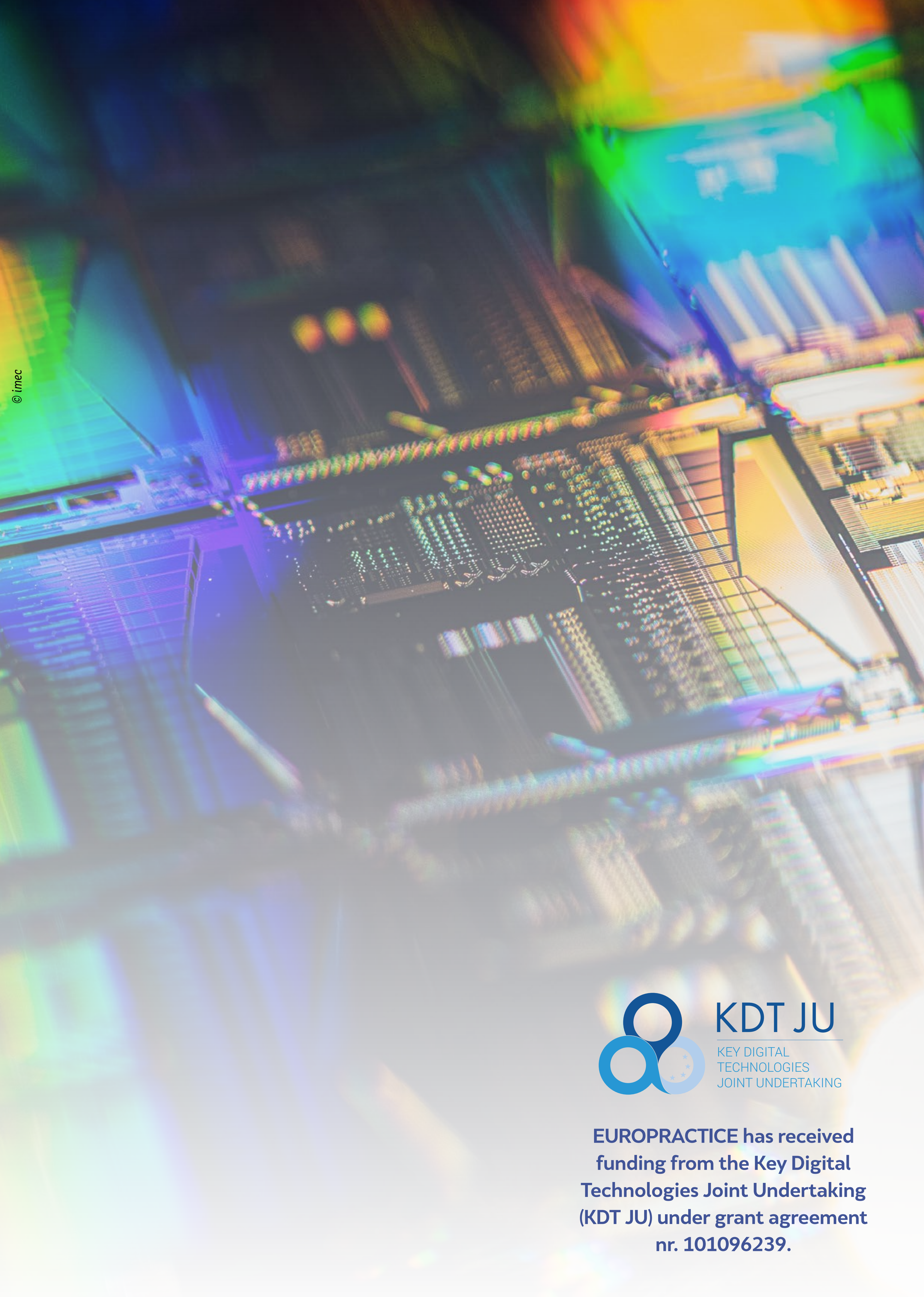

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