Chiplet & Packaging Co-Design EDA Tools

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Overview

GENIO™ is the only chiplet and package co-design EDA tool that integrates I/O planning, management and optimization for all 3DIC and Chiplet-based systems. Using GENIO™, designers quickly and easily assemble complete cross-domain systems (ICs and package), drive pin assignment, and optimize through a rule-based methodology.

GENIO™ integrates single or multiple high-pin count chiplets into a wide variety of package configurations, and supports wire-bond, flip-chip or mixed assembly designs.
Drag-and-drop functionality seamlessly creates the system directly in a graphic system view. With a common methodology, the system architect controls the design from either an IC-centric or package-centric perspective during early planning, prototyping, or detailed implementation.

One Step System Optimization

A 3D-aware cross-hierarchical pathfinding algorithm and methodology delivers one step interconnect optimization throughout the entire system hierarchy, from level 0 (PCB) to level n, supporting an unlimited number of hierarchy levels. Automated underlying algorithms reduce signal congestion and shorten the interconnections, providing significant benefits for pin assignment optimization and wire lengths/crossovers reduction that results in an extremely efficient use of routing resources.

A unique dedicated cockpit, showing the list of available system interconnect paths and sub-paths, allows the designers to interactively set-up constraints across design disciplines to drive system optimization.

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The **GENIO™** "What & Where" approach defines signal & pin groups to drive optimization on restricted portions of the design and establishes a priority between groups in the presence of constraints, ensuring the best possible signal arrangement.

GENIO™ supports all system architectures (2D, 2.5D, 3D configurations), all assembly styles (wire-bonding, flip-chip, and mixed) and all design flows (die-driven, package-driven, a mixture of top-down & bottom-up).

Key Features

- Chiplet-based system-level architectural exploration
- "What if" analysis & early feasibility studies avoid "dead-end" architecture
- Delivers "concept" design phase, before physical implementation starts
- I/O Planning & Interconnect optimization
- Creates/manages the physical relationship and hierarchy between components
- Cross-Hierarchical 3D-aware pathfinding
- Eliminates error prone manual activities associated with complex, horizontal and vertical, interconnects
- 2D & 3D interactive preview of entire/subsets of the assembled system including wire-bond/routing fly-lines
- Stores all cross-fabric structures in a common database
- Supports all major EDA standard formats and proprietary/custom formats through dedicated plug-ins

The GENIO™ Product Family

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❑ GENIO™ 2D

Supports 2D system architectures with one chip in a package, different assembly styles (wire-bonding or flip-chip) and flows (die-driven, package-driven or mixed).

❑ GENIO™ 2.5D

Provides a common environment to represent 2.5D systems that may include one or more die, stacked and/or side-by-side, silicon interposer, package and PCB portions along with design constraints. Flip-chip or mixed flip-chip/wire-bonding assembly can be die-driven, package-driven or a mix of the two.

Creates a floor-planning aware silicon interposer (including silicon bridges and AIB), design-ready for back annotation to place & route tools.

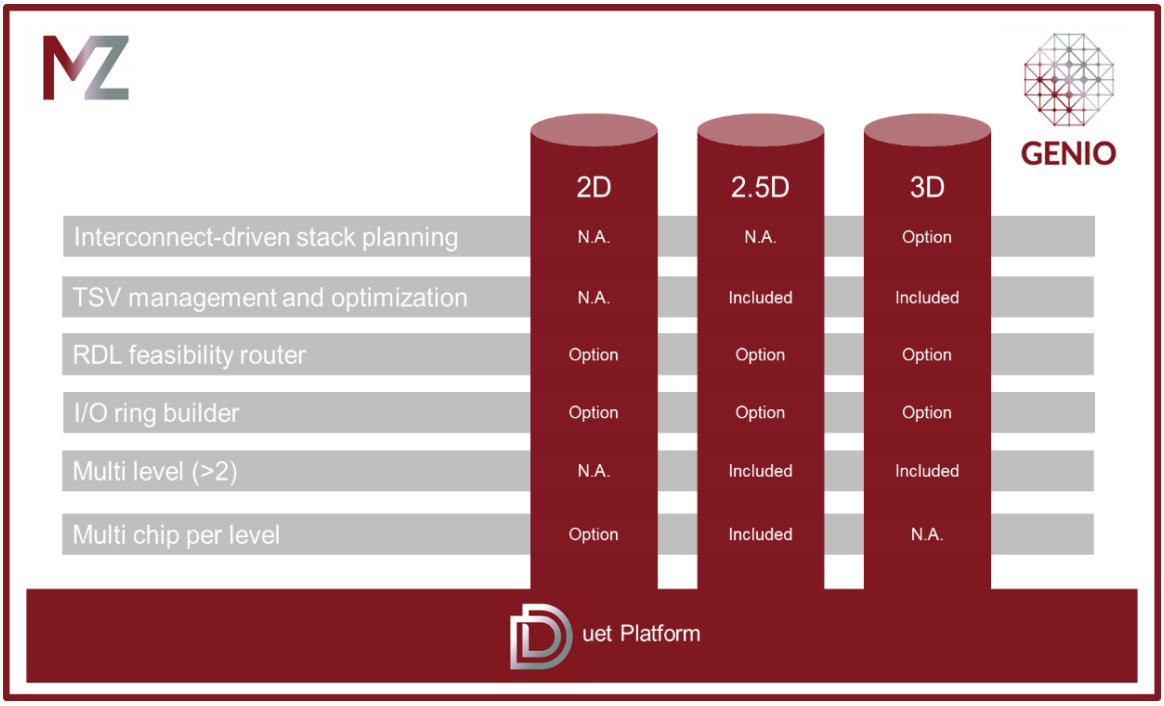
❑ GENIO™ 3D

Supports 3D stacking with an unlimited number of hierarchy levels, different assembly styles (wire-bonding, flip-chip or a mix) and flows (die-driven, package-driven or mixed).

❑ GENIO™ Combo

Delivers all the features available in 2D, 2.5D and 3D products.

The GENIO™ Product Family



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